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Colour Difference Amplifiers using the BF179 Transistor

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Two complete colour difference amplifier circuits are described, employing BF179 high voltage video transistors in the output stages, with the output transistors base driven or emitter driven.

The circuits are designed to provide full drive voltages for the A63-11X picture tube grids, and to have a similar performance to each other in terms of signal handling and bandwidth.

Design procedure is given for the required values of collector load in the individual output stages, and the evaluation of the matrix resistor values.

In addition the circuits illustrate the use of BA145 diodes to ensure constant d.c. level at the picture tube grids.

INTRODUCTION

Two forms of colour difference amplifier circuit are described, both of which incorporate the high voltage video transistor BF179[*] in the output stages to provide red, green and blue colour difference signals to the grids of the colour picture tube.

The main difference between the two amplifiers is in the form of the signal drive to the BF179 output stages. In one circuit emitter drive is employed by means of a driver transistor in series d.c. connection with the output transistor, and the complete amplifier circuit contains seven transistors. In the other circuit, the output transistors are base driven by normal grounded emitter preamplifier stages, and the complete circuit contains six transistors.

In both amplifier designs, all the stages are part d.c. coupled to minimise any possible transient effects, and an overall d.c. feedback system is employed to stabilise the transistor operating conditions.

The circuits employ the BA145 clamping diodes to ensure constant d.c. conditions at the grids of the picture tube.

GENERAL CIRCUIT DESCRIPTION

The complete circuit diagrams for the amplifiers are shown in Figs. 1 and 4. Both have similar overall gains and are designed to accept the demodulated chrominance signal and provide full drive to the picture tube.

Picture Tube Requirements

The minimum and maximum peak-to-peak colour difference drive requirements are given below, for an A63-11X colour tube with the cut-off voltage adjusted to 110V (Ref. 1):

$E_R'-E_Y'$ drive volts = 158 to 185V
$E_G'-E_Y'$ drive volts = 82 to 102V
$E_B'-E_Y'$ drive volts = 174 to 218V.

This range of drive adjustments can be provided by low wattage preset potentiometers in the collector loads of the BF179 transistors. Figs. 1 and 4 show that the collector load systems for the $R'-Y'$, $G'-Y'$ and $B'-Y'$ output stages are identical.

Colour difference signals are characterised by positive- and negative-going waveforms, hence the output stages are biased in class A conditions. It is shown later in *Choice of Output Stage Collector Load* (page 263) that with the bandwidth required for colour difference signals a collector load resistance of 10kΩ is satisfactory with high frequency compensation. Therefore, the minimum standing collector current in the output stages for full drive across the nominal 10kΩ collector load resistance is given by:

Signal $E_R'-E_Y'$ = 185V p-p, therefore I_c min =

$$\frac{185}{2\times 10\,000} = 9{\cdot}25\text{mA} \quad \ldots(1)$$

Signal $E_G'-E_Y'$ = 102V p-p, therefore I_c min = 5·1mA ...(2)

Signal $E_B'-E_Y'$ = 218V p-p, therefore I_c min = 10·9mA ...(3)

Calculation of Resistors in Collector Load Networks

In the circuits (Figs. 1 and 4) considerable use is made of divided collector loads both in the output stages and the preamplifier stages. The use of this system gives important operating advantages:

(i) it protects the transistor against the full effect of possible surge voltages after switching on the supply,
(ii) it prevents the full value of h.t. supply being applied to the collector of the transistor if the stage is momentarily cut off in an overdrive condition,
(iii) it avoids unnecessary current drain through a transistor when using a relatively low collector voltage compared with the supply voltage and a low value collector resistance.

Appendix 1 contains the derivation of the values of R_1 and R_2 (Fig. 9) in terms of collector voltage V_c, collector current I_c, supply voltage V_b, and equivalent load resistance R_L. Normally these values will be known and hence R_2 and R_1 are respectively given by:

$$R_2 = \frac{V_bR_L}{V_b-V_c-(I_cR_L)} \quad \ldots(4)$$

and

$$R_1 = \frac{R_2R_L}{R_2-R_L}. \quad \ldots(5)$$

Also the current in R_2 is given by:

$$I_{R2} = \frac{V_c[V_b-V_c-(I_cR_L)]}{V_bR_L}. \quad \ldots(6)$$

EMITTER DRIVEN COLOUR DIFFERENCE AMPLIFIER

In Fig. 1 the transistor stages TR_1 and TR_2 accept the weighted signals from the output of the $R'-Y'$ and $B'-Y'$ chrominance demodulators, the amplitude level of the $R'-Y'$ signal being nominally 0·5V p-p signal (Ref. 1).

The transistor stages TR_1 and TR_2 are designed to give similar gains into the respective bases of TR_3 and TR_4. TR_5 and TR_6, emitter driven by TR_3 and TR_4 respectively, form the $R'-Y'$ and $B'-Y'$ output stages. In the emitter circuits of TR_3 and TR_4 is the resistive matrix circuit which sums a portion of each of the $R'-Y'$ and $B'-Y'$ signals to produce a resultant $G'-Y'$ signal which is applied to the emitter driven $G'-Y'$ output stage.

The nominal supply voltages in the design are:

(i) 285V for the collector circuit of the output transistors,
(ii) 20V for base biasing and the collector circuits of the preamplifier stages.

As TR_3, TR_5 and TR_4, TR_6 are in series d.c. connection, the base bias on TR_5 and TR_6 determines the value of collector-emitter voltage across TR_3 and TR_4, whereas the bias voltage on the bases of TR_3 and TR_4 together with the voltage across the emitter resistors determines the standing collector current.

Choice of Output Stage Collector Load

The measured shunt capacitance from collector to earth is about 35pF for each of the output stages. This capacitance is made up as follows:

(i) transistor output capacitance plus heatsink about 8pF
(ii) clamp diodes and associated circuit about 12pF
(iii) input capacitance at grid of picture tube about 8pF
(iv) picture tube connections and general stray capacitance about 7pF.

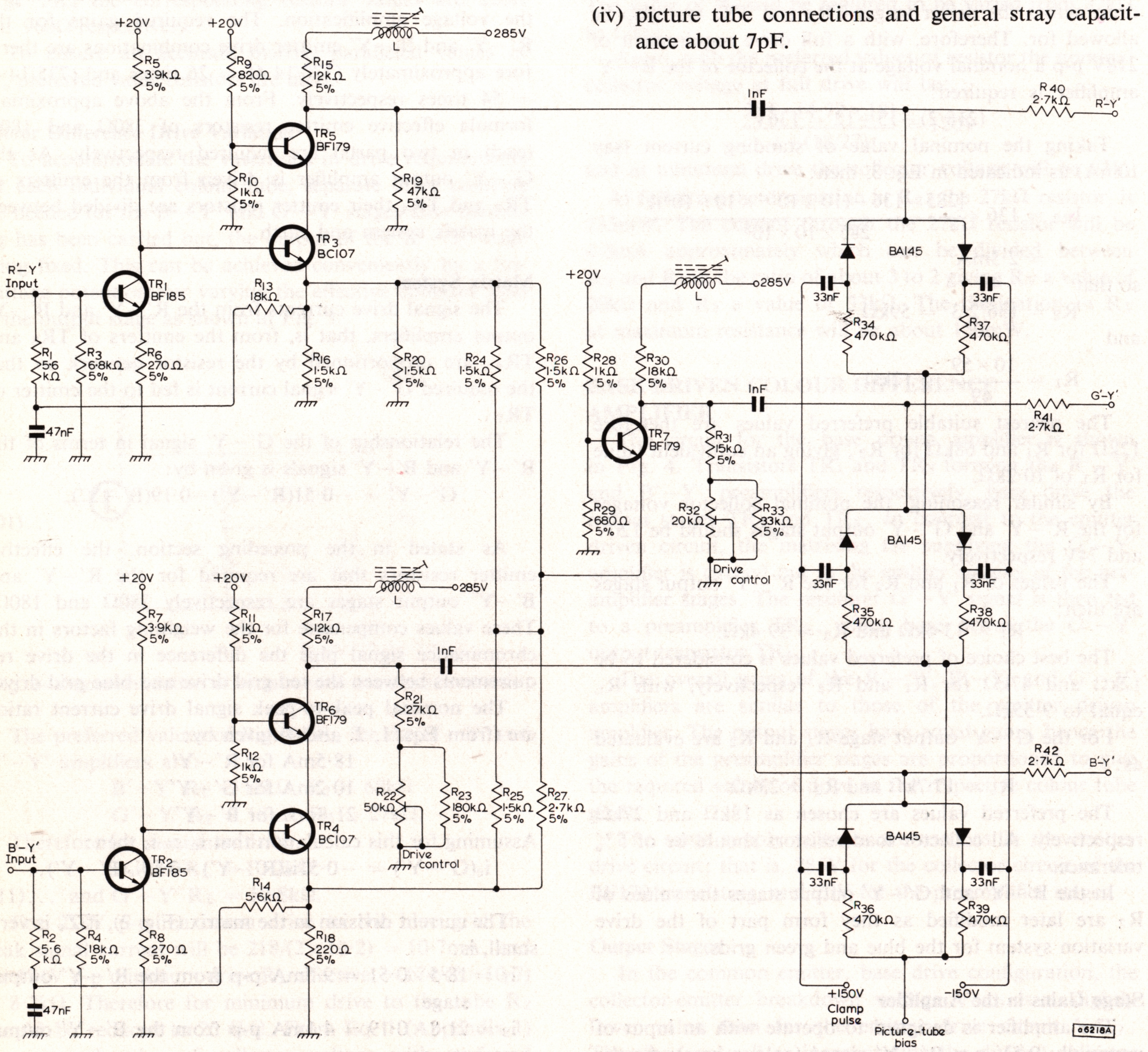

Fig. 1—Emitter drive circuit

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[*] A package (type 40822) of three BF179 output transistors is now available with the turnover voltages selected to suit the requirements of the three output stages.

With a 10kΩ load resistance in the collector of the output stage, the uncompensated rise time from 10% to 90% is given by:

$$\tau = 2{\cdot}2R_LC_{out} = 770\text{ns} \qquad \ldots(7)$$

To improve the rise time of the output circuit, a simple shunt-peaking circuit is used. The required inductance is given by:

$$L_1 = mR_L{}^2C_{out} \qquad \ldots(8)$$

where the factor m is related to the amount of overshoot in the network.

Values of m from 0·42 to 0·5 will give values for the inductance L varying from 1·47 to 1·75mH which can be incorporated in a tunable ferrite-cored coil. The higher inductance value gives a rise time improvement approaching 2 to 1 but with about 10% overshoot. With a measured rise time of approximately 500ns for the complete amplifier a satisfactory square wave output is given. This value corresponds to a 3dB cut-off frequency of about 700kHz.

The values of the divided load resistance (R_1 and R_2, Fig. 9) are derived from Eqs. 4 and 5. The h.f. knee voltage for the BF179 transistor is about 15V. A 12V potential drop across the driver stages TR_3 and TR_4 can also be allowed for. Therefore, with a full drive requirement of 218V p-p a nominal voltage at the collector of the B′−Y′ amplifier is required:

$$(218/2)+15+12 = 136\text{V}.$$

Taking the nominal value of standing current (say 10mA) as indicated in Eq. 3, then:

$$I_{R2} = 136\times\frac{[285-136-(10\times10^{-3}\times10\times10^3)]}{285\times10\times10^3}$$

$$= 2{\cdot}3\text{mA}$$

so that

$$R_2 = 136/2{\cdot}3 = 59\text{k}\Omega,$$

and

$$R_1 = \frac{10\times59}{49} = 12\text{k}\Omega.$$

The nearest suitable preferred values are therefore 12kΩ for R_1 and 68kΩ for R_2, giving an equivalent value for R_L of 10·2kΩ.

By similar reasoning, the nominal collector voltages for the R′−Y′ and G′−Y′ output stages should be 120V and 74V respectively.

The values of R_1 and R_2 for the R′−Y′ output stages are then:

$$R_1 = 13{\cdot}4\text{k}\Omega \text{ and } R_2 = 39{\cdot}4\text{k}\Omega.$$

The best choice of preferred values is considered to be 12kΩ and 47kΩ for R_1 and R_2 respectively, with R_L equal to 9·55kΩ.

For the G′−Y′ output stage R_1 and R_2 are evaluated as:

$$R_1 = 17{\cdot}7\text{k}\Omega \text{ and } R_2 = 23\text{k}\Omega.$$

The preferred values are chosen as 18kΩ and 27kΩ respectively. All collector load resistors should be of 5% tolerance.

In the B′−Y′ and G′−Y′ output stages the values of R_2 are later modified as they form part of the drive variation system for the blue and green grids.

Stage Gains in the Amplifier

The amplifier is designed to operate with an input of nominally 0·5V p-p R′−Y′ signal (colour bars). As the maximum drive output voltage is 185V p-p, the overall gain required in the R′−Y′ channel is nominally 370 times. The weighted signals from the R′−Y′ and B′−Y′ chrominance detectors are supplied in the ratio of 1/1·14 to 1/2·03, and the maximum drive output voltage required is 218V p-p from the B′−Y′ output stage. The maximum overall gain in the B′−Y′ channel is therefore:

$$2{\cdot}03/1{\cdot}14\times218/185\times370 = 775 \text{ times.}$$

The voltage gains of the first stages (TR_1 and TR_2) are approximately given by:

$$\frac{h_{fe}R_L}{h'_{ie}(1+h_{fe}R_e/h'_{ie})} \qquad \ldots(9)$$

where h'_{ie} and h_{fe} are the input resistance and current gain respectively. If $h_{fe}R_e \gg 1$ then the low frequency voltage gain approximates to the ratio of the collector load to the unbypassed emitter resistor. Therefore, the first stage gains of TR_1 and TR_2 are approximately 3900/270 = 14·4 times. The measured value was 13·5 times.

In the emitter drive circuit proper, TR_3 and TR_4 give the a.c. signal current control, whereas TR_5 and TR_6 give the voltage amplification. The required gains for the R′−Y′ and B′−Y′ emitter drive combinations are therefore approximately (370/14·4) = 26 times and (775/14·4) = 54 times respectively. From the above approximate formula effective emitter resistors of 380Ω and 180Ω (each in two parts) are required respectively. As the G′−Y′ output amplifier is driven from the emitters of TR_3 and TR_4 their emitter resistors are divided between the matrix system and earth.

Matrix System

The signal drive currents from the R′−Y′ and B′−Y′ output amplifiers, that is, from the emitters of TR_3 and TR_4, are proportioned by the resistor network so that the required G′−Y′ signal current is fed to the emitter of TR_7.

The relationship of the G′−Y′ signal in terms of the R′−Y′ and B′−Y′ signals is given by:

$$G'-Y' = -0{\cdot}51(R'-Y')-0{\cdot}19(B'-Y'). \qquad \ldots(10)$$

As stated in the preceding section, the effective emitter resistors that are required for the R′−Y′ and B′−Y′ output stages are respectively 380Ω and 180Ω. These values compensate for the weighting factors in the chrominance signal plus the difference in the drive requirements between the red grid drive and blue grid drive.

The nominal peak-to-peak signal drive current ratios are (from Eqs. 1, 2, and 3) given by:

18·5mA for R′−Y′
10·2mA for G′−Y′
21·8mA for B′−Y′.

Assuming for this calculation that $i_e \simeq i_c$ then:

$$i_e(G'-Y') = -0{\cdot}51i_e(R'-Y')-0{\cdot}19i_e(B'-Y'). \qquad \ldots(11)$$

The current division in the matrix (Fig. 2), if Z_e is very small, is:

$i_1 = 18{\cdot}5\times0{\cdot}51 = 9{\cdot}5$mA p-p from the R′−Y′ output stage

$i_2 = 21{\cdot}8\times0{\cdot}19 = 4{\cdot}1$mA p-p from the B′−Y′ output stage.

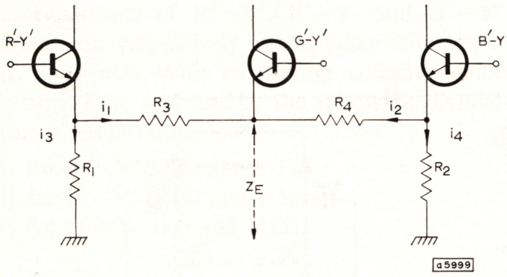

Fig. 2—Current division in the matrix

Therefore, in the peak-to-peak signal of 18·5mA for the R′−Y′ output stage, 9·5mA p-p is fed through the matrix and 9·0mA through the emitter resistor of TR_3. Similarly for the B′−Y′ output stage 4·1mA p-p is fed through the matrix, and 17·7mA p-p through the emitter resistor of TR_4.

Hence the required emitter resistor of TR_3 is given by 380×18·5/9·0 = 780Ω and the corresponding matrix resistor is 380×18·5/9·5 = 740Ω. For the B′−Y′ output stage TR_4 the corresponding resistor values are 220Ω and 960Ω respectively.

To ensure an accurate matrix, paralleled values of 5% preferred value resistors are used.

Colour Difference Drive Variation

To accommodate the variations in drive requirements for each individual colour tube, separate drive controls are needed for the B′−Y′ and G′−Y′ stages after matrixing has been carried out, the output of the R′−Y′ stage being fixed. This can be achieved conveniently by a low wattage potentiometer varying the effective collector load in the output stage as shown in Fig. 3.

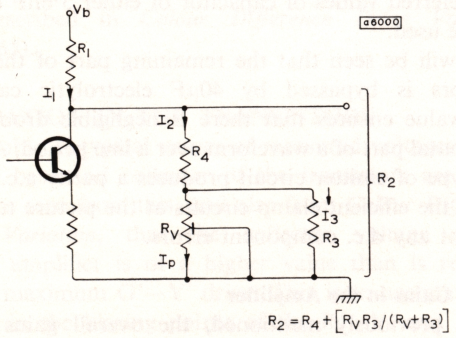

Fig. 3—Accommodation of variations in drive requirements

The preferred values of R_1 and R_2 for the B′−Y′ and G′−Y′ amplifiers are:

B′−Y′ R_1 = 12kΩ, R_2 = 68kΩ
G′−Y′ R_1 = 18kΩ, R_2 = 27kΩ.

Therefore for maximum drive

B′−Y′ R_L = 10·2kΩ
and G′−Y′ R_L = 10·8kΩ.

For 218V p-p maximum drive to the blue grid the peak signal current will be 218/(2×10·2) = 10·7mA, and for 174V p-p minimum drive R_L effective = 174/(2×10·7) = 8·2kΩ. Therefore for minimum drive to the tube R_2 should be reduced to 25·6kΩ. From Eq. 1 (Appendix 1) the nominal value of collector voltage with preferred values of resistor at maximum drive will be:

$$V_c = \frac{285-(10{\cdot}7\times12{\cdot}0)}{1+(12/68)} = 133\text{V}.$$

This gives a dissipation in the 68kΩ resistor of $133^2/(68\times10^3)$ = 270mW.

Again, V_c for minimum drive is nominally equal to:

$$V_c = \frac{285-(10{\cdot}7\times12{\cdot}0)}{1+(12/25{\cdot}6)} = 107\text{V}.$$

The dissipation in the 25·6kΩ resistor will thus be

$$107^2/(25{\cdot}6\times10^3) = 447\text{mW}.$$

When R_2 = 68kΩ, I_2 will be 1·96mA and this current can therefore be divided between R_V and R_3 (Fig. 3) in the ratio 3·6:1. This gives values of 50kΩ for R_L and 180kΩ for R_3 with 27kΩ preferred value for R_4. When R_V is maximum the dissipation is about 117mW, which is within the dissipation capabilities of a carbon track preset potentiometer.

Similarly, for the G′−Y′ output stage R_L = 10·8kΩ and the peak signal current required is 102/(2×10·8) = 4·72mA. For minimum drive R_L = 82/(2×4·72) = 8·7kΩ. The value of R_2 will be required to be varied from 27kΩ to 17kΩ.

Again, with the preferred values of resistor the nominal collector voltage at full drive will be:

$$\frac{285-(4{\cdot}72\times18)}{1+(18/27)} = 120\text{V}$$

and at minimum drive the collector voltage will be 97V.

At full drive the dissipation in R_2, the 27kΩ resistor, is 533mW. The current through the 27kΩ resistor will be 4·5mA approximately which can be divided between R_V and R_3 in the ratio of about 3 to 2 giving R_V a value of 20kΩ and R_3 a value of 33kΩ. The dissipation in R_V at maximum resistance will be about 150mW.

BASE DRIVEN COLOUR DIFFERENCE AMPLIFIER

The circuit for the base driven amplifier is shown in Fig. 4. Transistors TR_1 and TR_3 forming the R′−Y′ and B′−Y′ preamplifiers respectively, base drive the output stages TR_4 and TR_6. In contrast to the emitter driven circuit, the matrixing for supplying the G′−Y′ amplifier is carried out in the emitter circuits of the preamplifier stages. The resultant G′−Y′ signal is then fed to a preamplifier TR_2, which base drives the G′−Y′ output transistor TR_5.

The overall gains of the R′−Y′, B′−Y′ and G′−Y′ amplifiers are similar to those of the emitter driven amplifier. The output stages have equal gains, hence the gains of the preamplifier stages are proportioned to give the required values of drive to the respective colour tube grids.

The same supply voltages are used as in the emitter drive circuit; that is, 285V for the collector circuit of the BF179 transistors, and 20V for the preamplifier stages.

Output Stages

In the common emitter, base drive configuration, the collector-emitter breakdown voltage V_{CEO} is a slightly lower value than for the emitter drive circuit V_{CBO}. Therefore, as well as incorporating the divided collector

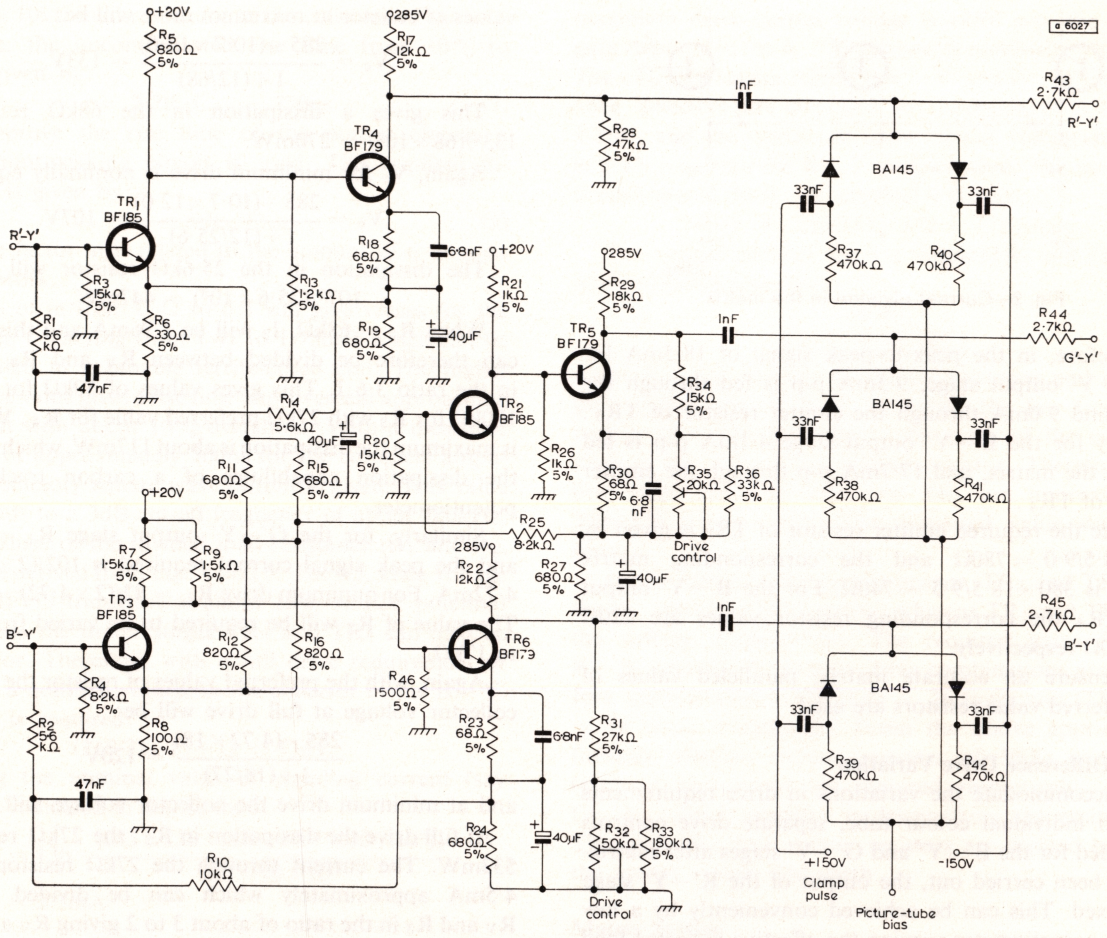

Fig. 4—Base drive circuit

load system of the emitter drive circuit, the effective base resistance is made as low as possible together with a low ratio of base resistance to emitter resistance.

An important characteristic of the base drive circuit is that of Miller effect on the coupling network between the preamplifier and output stages. This gives a reduction in the gain-bandwidth product of the amplifier as well as the output stage collector circuit. The BF179 has a feedback capacitance c_{re} of about 2·5pF typical, hence with a chosen gain of about 120 times for the output stages, the effective input capacitance of the BF179 will be about 300pF. This will produce a 3dB cut-off frequency point of about 1·1MHz for the 500Ω interstage coupling circuit.

In contrast to the shunt-peaking inductance as used in the emitter coupled output stage an emitter compensation C-R network is used as the main h.f. compensation. This arrangement is useful for h.f. compensation of the interstage circuit as well as the output stage collector circuit. Therefore, given $k = R_E C_E/R_L C_{out}$, where k is related to the rise time, then $C_{out} = 35$pF (*Choice of Output Stage Collector Load* page 263) $R_E = 68\Omega$ and $R_L = 10k\Omega$.

If k is taken as 1·2, which gives a small amount of overshoot, then the required value of emitter decoupling capacitor is given by:

$$C_E = (1{\cdot}2\times 35\times 10^4/68)\times 10^{-3} = 6{\cdot}2\text{nF}.$$

Preferred values of capacitor of either 5·6nF or 6·8nF can be used.

It will be seen that the remaining part of the emitter resistors is bypassed by 40μF electrolytic capacitors. This value ensures that there is negligible droop in the horizontal part of a waveform over a line period. Although this type of emitter circuit produces a partly a.c. coupled stage, the efficient clamp circuits at the picture tube grids prevent any d.c. component errors.

Stage Gains in the Amplifier

As previously mentioned, the overall gains for the R′−Y′ and B′−Y′ channels in the amplifier are 370 and 775 times. With the output stage gains of 120 times the preamplifier gains are therefore approximately 3 times and 6·4 times. The effective collector load resistance for the preamplifier stages is normally 500Ω, therefore from Eq. 9 the effective emitter resistors for the R′−Y′ and B′−Y′ preamplifier stages will be approximately 165Ω and 78Ω.

Divided collector loads are used for the preamplifier stages. Also the emitter current of the G′−Y′ preamplifier is considerably lower than in the R′−Y′ and B′−Y′ preamplifier stages to avoid undue influence of extra bias on these stages. The collector voltage of these amplifiers is dependent on the biasing condition of the output stage. Also, to relate with preferred values of resistors, the collector currents of R′−Y′, B′−Y′ and G′−Y′ preamplifiers are respectively set at approximately 9mA, 12mA, and 5mA. With an average collector voltage of 7·5V, from Eqs. 3, 4 and 5, the following divided load resistor values are obtained:

(i) for R′−Y′ 820Ω and 1·2kΩ
(ii) for B′−Y′ 750Ω and 1·5kΩ
(iii) for G′−Y′ 1kΩ and 1kΩ.

Matrix System

From Fig. 2:

$$i_1 = i_e(R'-Y')\frac{R_1}{R_3+R_1}$$

and

$$i_2 = i_e(B'-Y')\frac{R_2}{R_2+R_4}$$

where $i_1+i_2 = i_e(G'-Y')$;

also

$$R_E(R'-Y') = \frac{R_1R_3}{R_1+R_3} = 165\Omega$$

and

$$R_E(B'-Y') = \frac{R_2R_4}{R_2+R_4} = 78\Omega.$$

Hence from Eq. 11:

$$\frac{R_1}{R_3+R_1} = 0{\cdot}51 \text{ and } \frac{R_2}{R_2+R_4} = 0{\cdot}19.$$

Therefore, $R_3 = 165/0{\cdot}51$ and $R_4 = 78/0{\cdot}19$, giving $R_3 = 325\Omega$ and $R_4 = 410\Omega$. Correspondingly, $R_1 = 338\Omega$ and $R_2 = 96\Omega$. In the circuit the nearest preferred values are used, with resistors of 5% tolerance.

Drive Variation

The drive variation to the colour tube grids is similar to that described in *Colour Difference Drive Variation* (page 265).

DISSIPATION IN THE TRANSISTORS

In Table 1, typical values of measured voltages at the emitter, base and collector of the transistors are given. It will be seen from this, and also from *Colour Difference Drive Variation*, that the collector voltage of the G′−Y′ amplifier is of a higher value than is required for the maximum G′−Y′ drive. This is to accommodate spreads in the biasing points of the R′−Y′ and B′−Y′ amplifiers, slight variations in matrix values, as well as spreads in the biasing point of the amplifier. As a general rule the collector voltage for the R′−Y′ and B′−Y′ amplifiers under normal operating conditions should be about half that value when the collector approaches zero. With values of 47kΩ and 68kΩ, these voltages with zero collector current will be approximately 230V and 240V for a 285V supply. In addition to these conditions a voltage drop of between 5 and 10V should be allowed for collector leakage current in the load resistor.

The maximum rated dissipation of the BF179 transistor is 1·7W when fitted with a suitable heatsink. The relationship is:

$$P_c\ \text{max} = \frac{T_j-T_A}{R_{th}} \qquad \ldots(12)$$

where R_{th} = the thermal resistance. With maximum junction and ambient temperatures of 200°C and 55°C respectively R_{th} = 85degC/W. The thermal resistance between the junction and mounting base is given as 60degC/W, hence a heatsink of thermal resistance of not more than 25degC/W should be used for maximum dissipation. Without a heatsink the value of R_{th} is given as 220degC/W, therefore from Eq. 12 the maximum dissipation of the transistor is limited to 660mW. In Table 2 dissipation figures are indicated for the various transistors, and it is shown that the G′−Y′ output transistor will not normally require a heatsink.

TABLE 1

Measured Voltages in Circuits

$V_{b1} = 285V \quad V_{b2} = 20V$

Base Drive Circuit	TR_1	TR_2	TR_3	TR_4	TR_5	TR_6
Emitter Volts	3·0	3·4	1·45	7·2	6·9	8·0
Base Volts	3·7	4·1	2·2	7·6	7·3	8·2
Collector Volts	7·6	7·3	8·2	130	108	135

Emitter Drive Circuit	TR_1	TR_2	TR_3	TR_4	TR_5	TR_6	TR_7
Emitter Volts	0·8	1·1	7·2	3·2	10·6	9·5	7·6
Base Volts	1·5	1·8	7·7	3·8	11·0	10·0	8·0
Collector Volts	7·7	3·8	10·6	9·5	136	130	116

$V_{b1} = 313{\cdot}5V \quad V_{b2} = 22V$

Base Drive Circuit	TR_1	TR_2	TR_3	TR_4	TR_5	TR_6
Emitter Volts	3·4	3·5	1·65	8·3	7·6	8·8
Base Volts	4·0	4·3	2·3	8·6	7·9	9·0
Collector Volts	8·6	7·9	9·0	135	115	140

Emitter Drive Circuit	TR_1	TR_2	TR_3	TR_4	TR_5	TR_6	TR_7
Emitter Volts	0·9	1·25	7·6	3·4	11·8	10·5	8·2
Base Volts	1·6	1·95	8·3	4·0	12·0	11·0	8·8
Collector Volts	8·3	4·0	11·8	10·5	150	140	124

TABLE 2

Average Dissipation of Transistors with Nominal Supply Voltages of 285V and 20V

Base Drive Circuit	TR_1	TR_2	TR_3	TR_4	TR_5	TR_6
Dissipation mW	40	19·5	70	1245	560	1335

Emitter Drive Circuit	TR_1	TR_2	TR_3	TR_4	TR_5	TR_6	TR_7
Dissipation mW	18·5	11	34	63	1190	1260	550

Average Dissipation of Transistors with Supply Voltages of 285V+10% and 20V+10%

Base Drive Circuit	TR_1	TR_2	TR_3	TR_4	TR_5	TR_6
Dissipation mW	47	27	84	1525	725	1630

Emitter Drive Circuit	TR_1	TR_2	TR_3	TR_4	TR_5	TR_6	TR_7
Dissipation mW	25	12·5	40·5	82	1450	1610	685

CLAMP CIRCUITS

The d.c. restoration is provided by a double-diode clamp circuit as shown in Figs. 1 and 4. The circuit, which is of standard form, ensures constant level at the grids of the picture tube during the blanking period.

Equal and opposite clamping pulses of about 150V peak are applied to the 33nF capacitors. This level of clamp voltage ensures that the diodes remain in a non-conducting state between pulses for maximum signal drive voltage to the picture tube grid.

TEMPERATURE STABILITY

The collector voltage of each individual stage of the colour difference amplifiers was measured against an ambient temperature range of 20 to 55°C to give an indication of the temperature stability of the circuits. The results of these measurements are shown in Figs. 5, 6, 7 and 8. The variations of the respective collector voltages over the temperature range are a very small percentage of the nominal working voltage. The emitter drive circuit collector voltage of the BF179 in the G′−Y′ output stage shows the largest variation. This is because it also responds to the change in emitter voltage of the R′−Y′ and B′−Y′ output stages, as well as its own temperature spread. However, the nominal collector voltage of the G′−Y′ amplifier is of a large enough value to accommodate the variation.

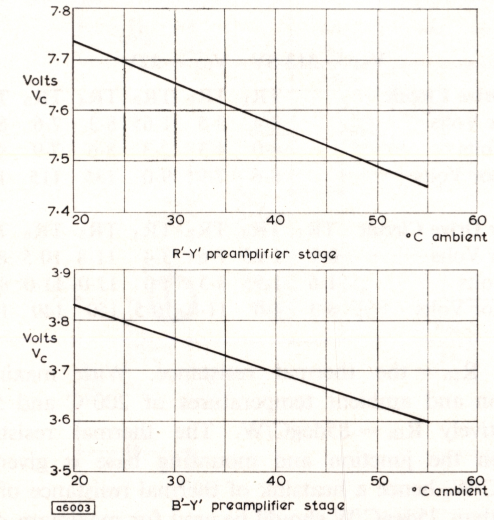

Fig. 5—Collector voltage as function of temperature for the R′—Y′ and B′—Y′ BF185 preamplifier stages in emitter drive circuit

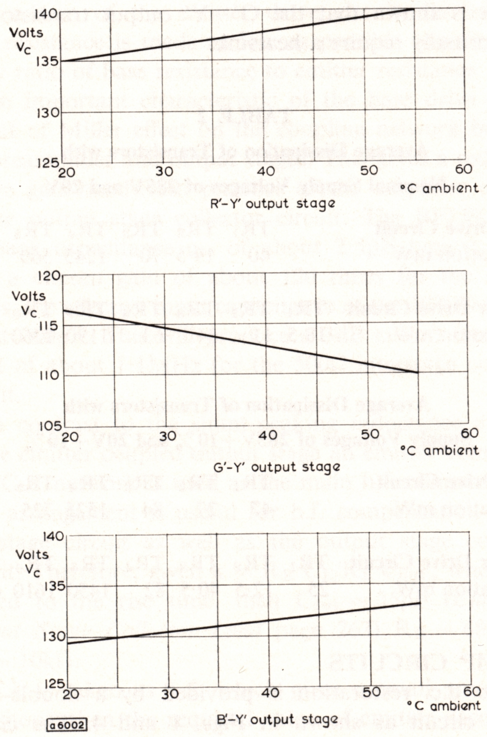

Fig. 6—Collector voltage as function of temperature for R′—Y′, G′—Y′ and B′—Y′ BF179 output stages in emitter drive circuit

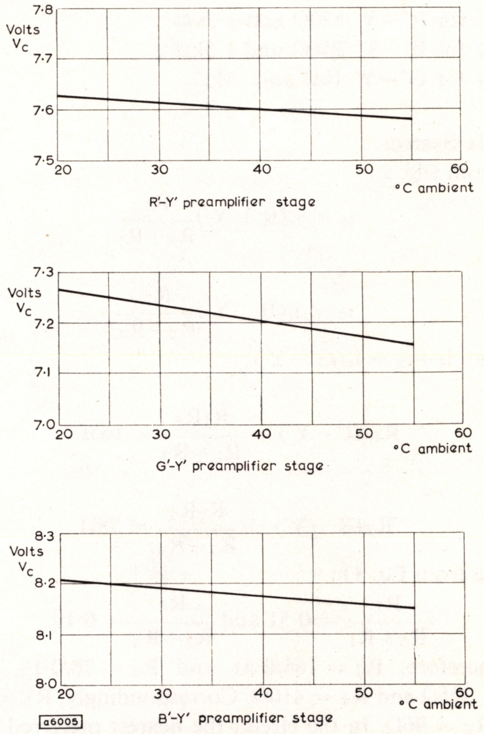

Fig. 7—Collector voltage as function of temperature for R′—Y′, G′—Y′ and B′—Y′ BF185 preamplifier stages in base drive circuit

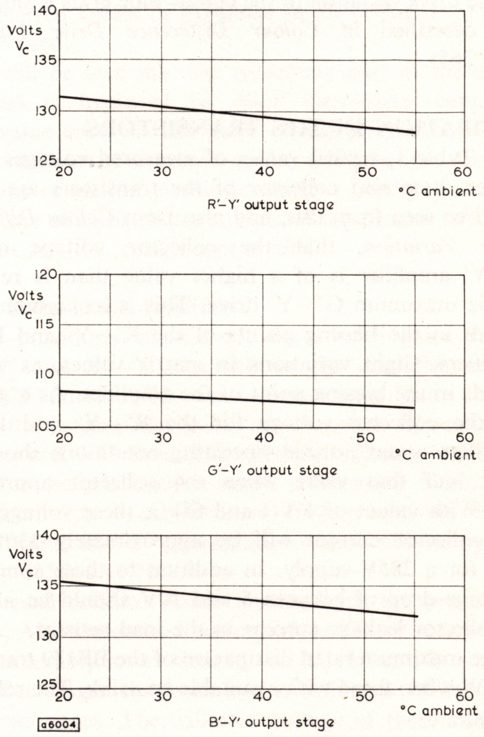

Fig. 8—Collector voltage as function of temperature for R′—Y′, G′—Y′ and B′—Y′ BF179 output stages in base drive circuit

REFERENCE

1. Hobbs, D. S., 'Hybrid Colour-difference Decoding Circuits'. **Mullard Technical Communications**, Vol. 9, No. 85, Jan. 1967, pp. 111 to 118, and see Vol. 9, No. 86, March 1967, p. 143.

APPENDIX 1

Derivation of the Values of R_1 and R_2 in the Divided Load Resistance

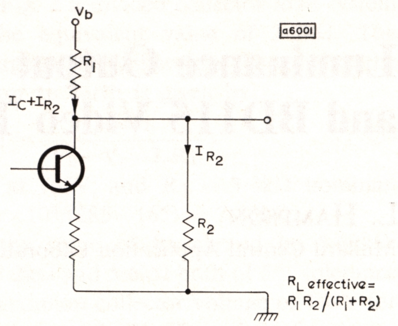

Fig. 9—Basic output circuit

Fig. 9 shows the following relationship:

$$V_c = V_b-(I_cR_1+I_{R2}R_1)$$

where

$$I_{R2} = V_c/R_2$$

and V_c, V_b and I_c are the collector voltage, supply voltage and collector current respectively. Therefore

$$V_c = V_b-(I_cR_1+V_cR_1/R_2)$$

or

$$V_c[1+(R_1/R_2)] = V_b-I_cR_1$$

giving

$$1+(R_1/R_2) = \frac{V_b-I_cR_1}{V_c}. \qquad \ldots(1)$$

Now

$$R_1 = \frac{V_b-V_c}{I_c+I_{R2}}$$

therefore

$$1+(R_1/R_2) = \frac{V_b-I_c(V_b-V_c)/(I_c+I_{R2})}{V_c}.$$

If this equation is divided through by R_1:

$$\frac{R_1+R_2}{R_1R_2} = \frac{V_b-I_c(V_b-V_c)/(I_c+I_{R2})}{V_cR_1}.$$

Now

$$R_L = R_1R_2/(R_1+R_2).$$

Hence

$$R_L = \frac{V_cR_1}{V_b-\frac{I_c(V_b-V_c)}{I_c+I_{R2}}}.$$

Substitution for R_1 gives:

$$\frac{V_c(V_b-V_c)}{I_c+I_{R2}} \Big/ V_b-\frac{I_c(V_b-V_c)}{I_c+I_{R2}}$$

$$= \frac{V_c(V_b-V_c)}{V_b(I_c+I_{R2})-I_c(V_b-V_c)}$$

or

$$R_L = \frac{V_c(V_b-V_c)}{V_bI_{R2}+V_cI_c}. \qquad \ldots(2)$$

Solving for I_{R2}:

$$I_{R2} = \frac{V_c[V_b-V_c-(I_cR_L)]}{V_bR_L}. \qquad \ldots(3)$$

Now

$$R_2 = V_c/I_{R2}$$

or

$$R_2 = \frac{V_bR_L}{V_b-V_c-(I_cR_L)} \qquad \ldots(4)$$

and

$$R_1 = \frac{R_LR_2}{R_2-R_L}. \qquad \ldots(5)$$

Luminance Output Stages using BF186 and BD115 Video Transistors

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The performances of the BF186 and BD115 transistors are examined in luminance output stages. Collector loads of 3·3kΩ and 2·2kΩ respectively are used with maximum dissipations of 2·5W and 4·0W. In each circuit the operating conditions, rise time, and frequency response of the amplifiers are evaluated.

A.C. coupling is used throughout the major part of the complete amplifiers, and the performances of a d.c. restorer and a driver clamp circuit are compared.

INTRODUCTION

The performances of the BF186 and BD115 transistors are examined in luminance output stages, for driving the cathodes of the A63–11X colour picture tube, as part of a complete colour difference drive system (Ref. 1). From the circuit standpoint the main differences between the BF186 and BD115 are in the power dissipation and voltage ratings. The power dissipation of the BF186 is 2·5W maximum with a 3·3kΩ collector load resistor and these parameters form a basis for design of the BF186 output stage. For the BD115 transistor a design is given using a nominal 2·2kΩ collector load resistor with a maximum power dissipation of about 4W and a correspondingly increased video bandwidth. Both circuits are designed for 625 lines only and provide sufficient video output voltage, that is to say about 105V black-to-white, to give the maximum required drive to the tube cathodes.

The circuits described in Ref. 1 are a.c. coupled, therefore, to maintain a continuity in circuit design, as well as for the practical advantages, a.c. coupling is used throughout the major part of the complete luminance amplifier, with appropriate d.c. restoration in the base of an emitter follower stage.

This article describes the relative performance of a simple d.c. restoration circuit and a driven clamp circuit, and compares their efficiencies in maintaining constant black level conditions within the range of contrast provided.

BF186 OUTPUT STAGE

The preamplifier stages in the complete luminance amplifier, as shown in Fig. 1, are similar to a previously published design (Ref. 2). This section contains the luminance delay line and take-off points for a.g.c. operation and subsequent sync separation. The output from the contrast control at point (A) is fed to the input points (A) as shown in either Fig. 2 or Fig. 4. These two circuits are similar except for the method of d.c. restoration. In Fig. 2 a single-diode d.c. restorer is used, with the lower end connected to the brightness control, whereas Fig. 4 contains a double-diode clamp circuit, also with the lower end connected to the brightness control.

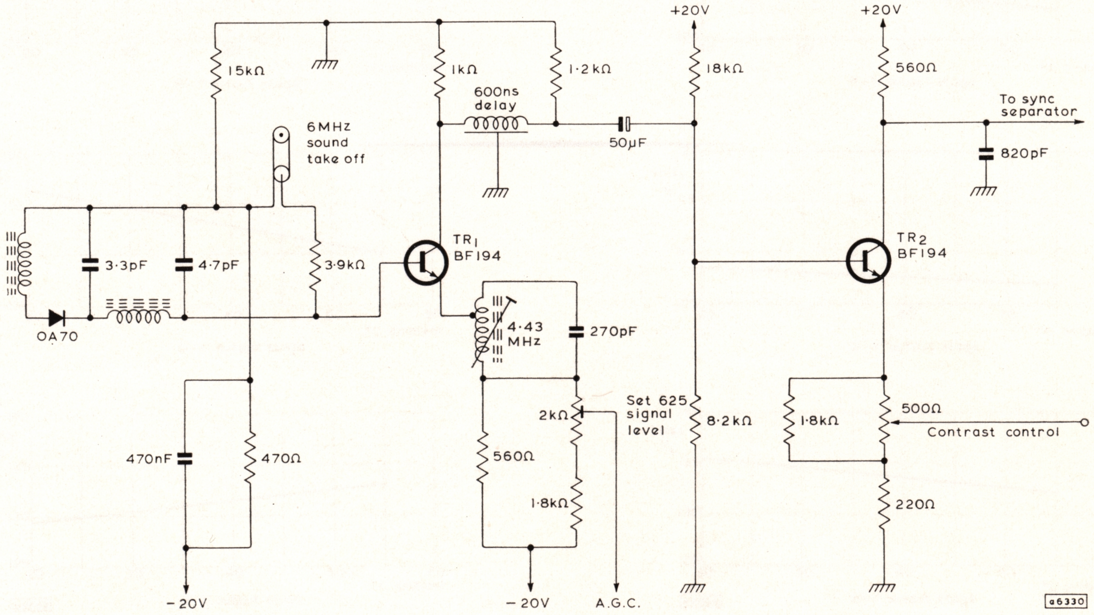
+20V
+20V
15kΩ
1kΩ
1·2kΩ
18kΩ
560Ω
600ns
delay
To sync
separator
6MHz
sound
take off
50μF
820pF
TR1
BF194
TR2
BF194
3·3pF
4·7pF
3·9kΩ
OA70
4·43
MHz
270pF
2kΩ
Set 625
signal
level
8·2kΩ
1·8kΩ
500Ω
Contrast control
A
470nF
470Ω
560Ω
1·8kΩ
220Ω
−20V
−20V
A.G.C.
a6330

Fig. 1—Video detector and preamplifier stages

The final preamplifier stage in the complete amplifier consists of an emitter follower using a BF185 which base drives the BF186 output stage. The emitter resistor of the BF185 represents a compromise in obtaining a high input impedance for the efficient operation of the d.c. restoration circuit and a low d.c. resistance for the base circuit of the output stage.

The output stage contains a low level blanking circuit, consisting of a BC148 transistor in series with the emitter resistor of the BF186. The collector circuit of the output stage includes a network for individual adjustment of the drive requirements to each cathode without affecting the d.c. level. The above two circuit arrangements have also been described previously (Ref. 2).

Operating Conditions of BF186

In the data sheets for the BF186 transistor the maximum dissipation is given as 2·5W, with a minimum collector emitter breakdown voltage of 165V. To be able to make full use of the available power dissipation at a nominal supply voltage it is permissible to operate the collector into the breakdown voltage region, at above nominal supply voltage, provided that the maximum dissipation is not exceeded.

With a nominal collector voltage and collector load of 165V and 3·3kΩ the power input to the transistor will be $(165)^2/4 \times 3{\cdot}3 \times 10^3 = 2{\cdot}06$W. Therefore to keep within the rated 2·5W the collector voltage should not exceed 182V, when component and supply voltage spreads are allowed for.

In the circuit of Fig. 2 a divided collector load system is used to form the equivalent value of 3·3kΩ. The nominal supply voltage is 285V, therefore the value of the resistor from collector to earth is given by,

$$R_2 = \frac{V_b R_L}{V_b - V_c - I_c R_L}\ . \qquad \ldots(1)$$

If $I_c R_L$ tends to 0 at 165V, and $R_L = 3{\cdot}3$kΩ nominal, then $R_2 = 285 \times 3{\cdot}3 \times 10^3/(285-165) = 7{\cdot}85$kΩ.

It follows that the value of R_1 should be 5·68kΩ. Preferred values of 8·2kΩ and 5·6kΩ both of 5% tolerance are used, giving a maximum collector voltage of 169V for a nominal supply voltage of 285V. The value of collector load when the above preferred values are used is 3·33kΩ.

Fig. 3 shows the operating conditions for the BF186 with the 3·3kΩ load resistor plotted on the $V_{CE}-I_c$ axes.

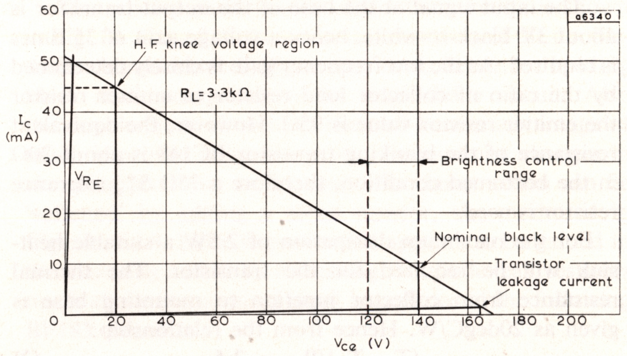

Fig. 3—Operating conditions for BF186 with a 3·3kΩ load resistor

It will be seen that from the maximum collector voltage of 169V the following must be subtracted:

(i) typically 4V due to leakage current through the collector load resistor,

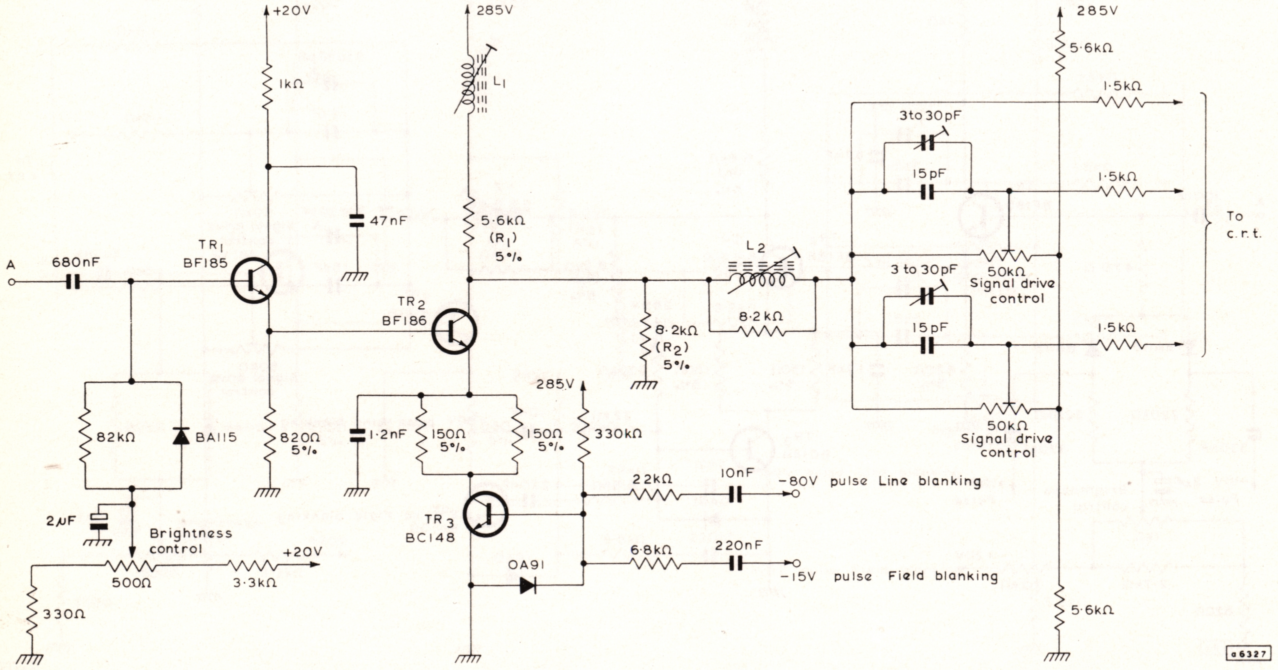
+20V
285V
285V
1kΩ
L1
5·6kΩ
47nF
5·6kΩ
(R1)
5%
1·5kΩ
3to30pF
15pF
1·5kΩ
To
c.r.t.
A
680nF
TR1
BF185
TR2
BF186
L2
8·2kΩ
(R2)
5%
8·2kΩ
3 to 30pF
50kΩ
Signal drive
control
15pF
1·5kΩ
82kΩ
BA115
820Ω
5%
1·2nF
150Ω
5%
150Ω
5%
285V
330kΩ
50kΩ
Signal drive
control
22kΩ
10nF
−80V pulse Line blanking
2μF
TR3
BC148
Brightness
control
+20V
6·8kΩ
220nF
−15V pulse Field blanking
OA91
500Ω
3·3kΩ
330Ω
5·6kΩ
a6327

Fig. 2—Emitter follower driver stage with single-diode d.c. restoration, and BF186 luminance output stage

(ii) typically 20V for the h.f. knee voltage of the transistor,
(iii) approximately 4V across the emitter resistor at maximum current excursion (that is, operation in the knee of the transistor).

This leaves, therefore, approximately 140V available to accommodate the video signal, which can be divided as follows:

(i) 105V black-to-white signal for maximum tube drive,
(ii) 20V shift for brightness control,
(iii) 15V for blanking.

Black level is set nominally at 140V, therefore with a typical tube cut-off of 110V, the bias at the grids is set at 30V. At maximum contrast and brightness setting the peak white signal will be operating into the h.f. knee voltage region.

The input signal at the base of the output transistor is about 3V black-to-white, hence a voltage gain of 35 times is required. As the low frequency gain is closely determined by the ratio of collector load resistor to emitter resistor the emitter resistor value is 95Ω. However, the equivalent resistance of the blanking transistor BC148 is about 20Ω in the bottomed condition, therefore a 75Ω 5% tolerance resistor is used.

For the maximum dissipation of 2·5W a suitable heatsink will be required for the transistor. The thermal resistance from collector junction to mounting base is given as 20degC/W. Hence from the relationship:

$$(T_j - T_A)/R_{th} = 2{\cdot}5 \qquad \ldots(2)$$

where junction and ambient temperatures are 200°C and 55°C maximum, the total thermal resistance R_{th} is 58deg C/W. A heatsink with a thermal resistance of not greater than 38degC/W is required.

H.F. Compensation of BF186 Output Stage

To approach an acceptable video bandwidth in the output stage, normal h.f. compensation is required. In the uncompensated amplifier with the 3·3kΩ collector load, the measured rise time (10% to 90% of the output waveform) was 340ns, which corresponds to a 3dB cut-off frequency of 1·03MHz. Hence the total shunt capacitance in the collector output circuit amounts to 47pF. To obtain the maximum h.f. compensation, shunt-series-peaking coils are used in the collector circuit and emitter compensation is applied, as shown in Fig. 2.

The total capacitance consists of:

(i) transistor output capacitance, plus heatsink capacitance	10pF,
(ii) self capacitance of collector load resistors, plus stray wiring capacitance	5pF,
(iii) input capacitance of picture tube cathodes,	17pF,
(iv) capacitance of drive potentiometer system plus wiring capacitance	15pF.

Sections (i and ii) and (iii and iv) are arranged in a ratio of 1:2 for which design formulas have been given (Ref. 3). To obtain the optimum frequency response in the output stage the values of the shunt and series inductances were derived for an approximate 'linear phase' condition and the final output waveform with about 5% overshoot was derived with emitter compensation.

If capacitances (i and ii) are C_T, and (iii and iv) C_P then the ratio $\alpha = C_T/(C_T+C_P) = 0{\cdot}32$.

If values are taken for $m_1 = 0{\cdot}1$ for the shunt inductance and $m_2 = 0{\cdot}46$, where $m = L/R_L^2(C_T+C_P)$, then the values of the shunt and series inductances L_1 and L_2 in microhenrys become:

$$L_1 = 0{\cdot}1 \times 3{\cdot}3^2 \times 47 = 52\mu H$$

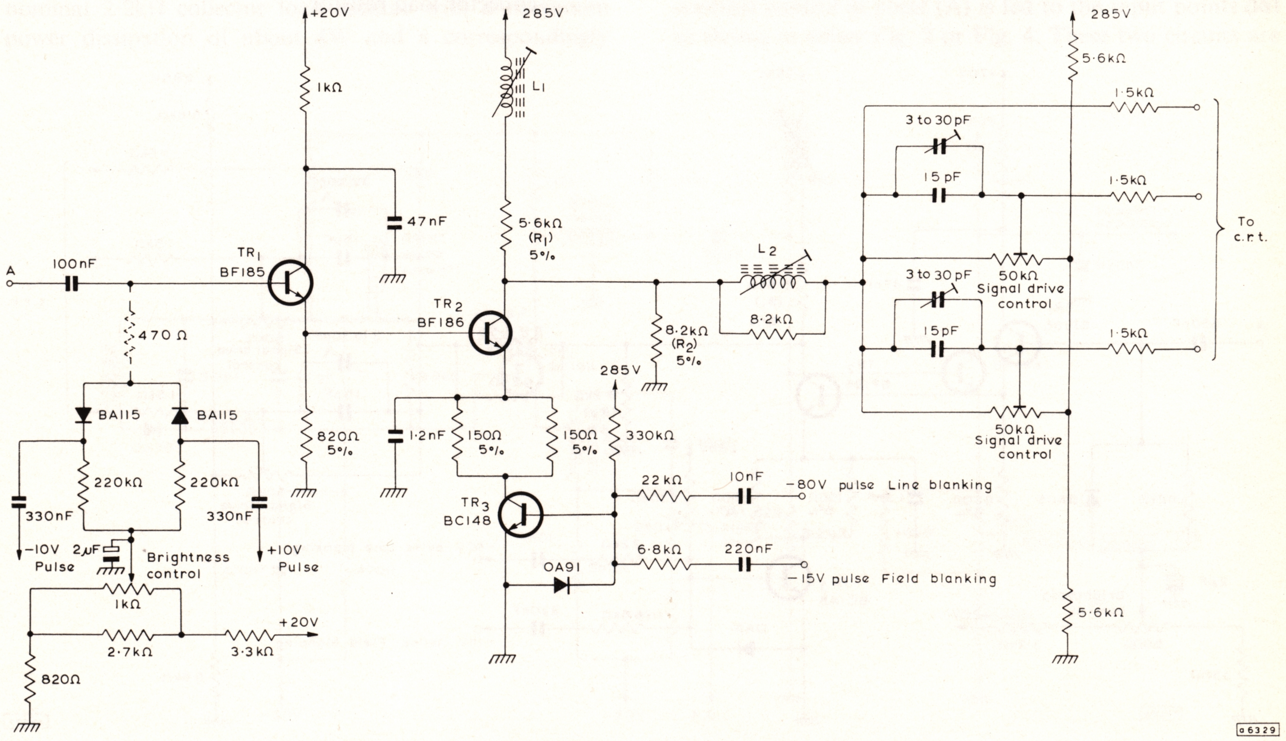
+20V
1kΩ
47nF
A
100nF
TR1
BF185
470 Ω
BA115
BA115
220kΩ
220kΩ
330nF
330nF
-10V Pulse
2μF
Brightness control
+10V Pulse
1kΩ
2·7kΩ
3·3kΩ
+20V
820Ω
820Ω 5%
285V
L1
5·6kΩ (R1) 5%
TR2
BF186
1·2nF
150Ω 5%
150Ω 5%
285V
330kΩ
TR3
BC148
22 kΩ
10nF
-80V pulse Line blanking
6·8kΩ
220nF
-15V pulse Field blanking
OA91
L2
8·2kΩ
8·2kΩ (R2) 5%
3 to 30pF
15 pF
50kΩ Signal drive control
1·5kΩ
To c.r.t.
5·6kΩ
66329

Fig. 4—Emitter follower driver stage with double-diode clamp, and BF186 luminance output stage

and $L_2 = 0{\cdot}46 \times 3{\cdot}3^2 \times 47 = 235\mu H$.

In the emitter compensation circuit a value of 1·2nF was chosen as a suitable value giving the relationship $k = R_E C_E / R_L(C_T+C_P) = 0{\cdot}74$. By reducing L_2 to about 190μH and applying a damping resistor of 8·2kΩ, an average rise and fall time for the output stage of 120ns was obtained. This corresponds to a 3dB bandwidth of about 3MHz. The measured frequency response of the output stage is shown in Fig. 5; the 3dB bandwidth is in excess of 3MHz.

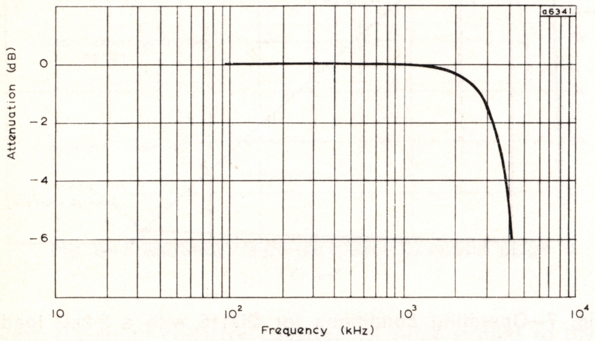

Fig. 5—Frequency response of BF186 output stage

Emitter Driver Stage

A BF185 transistor is used as the driver stage for the BF186 output transistor. At the nominal black level condition the base voltage of the output transistor is approximately 1·6V. The current in the driver transistor is therefore approximately 2mA. The collector circuit contains a load resistor of 1kΩ which limits the dissipation in the transistor to about 100mW.

The product of the current gain ($h_{fe} = 100$) and the emitter resistor, gives the driver stage a high input impedance suitable for the operation of d.c. restoration in the base circuit.

D.C. Restoration

Fig. 2 shows the emitter driver stage with single-diode restoration. The BA115 rectifies the tips of the sync pulses and provides positive bias for the base of the BF185. The brightness control current is fed to the base via the 82kΩ resistor.

In Fig. 4 the emitter driver stage has d.c. restoration provided by means of a double-diode clamp circuit. The required positive- and negative-going keying pulses are 10V peak, from a low-impedance source, and operate the clamp circuit on the back porch of the sync pulse.

The relative performance of the two circuits is shown in Fig. 10. For a 7:1 change in contrast control the double-diode clamp circuit is about four times better for holding black level, compared to the single-diode circuit. Also the double-diode circuit has the well-known advantage of much improved noise immunity. To minimise changes in clamping level due to h.f. noise the clamp action can be 'softened' by adding a series resistor, shown dotted in Figs. 4 and 8. Little improvement appears to be gained in the clamping action by increasing the diode leak resistors much above the nominal input impedance of the following BF185 transistor.

BD115 OUTPUT STAGE

The circuits for the BD115 output stage are shown in Fig. 6 and Fig. 8. They are similar to the circuits for the BF186, except that the BD115 collector load is reduced to 2·2kΩ.

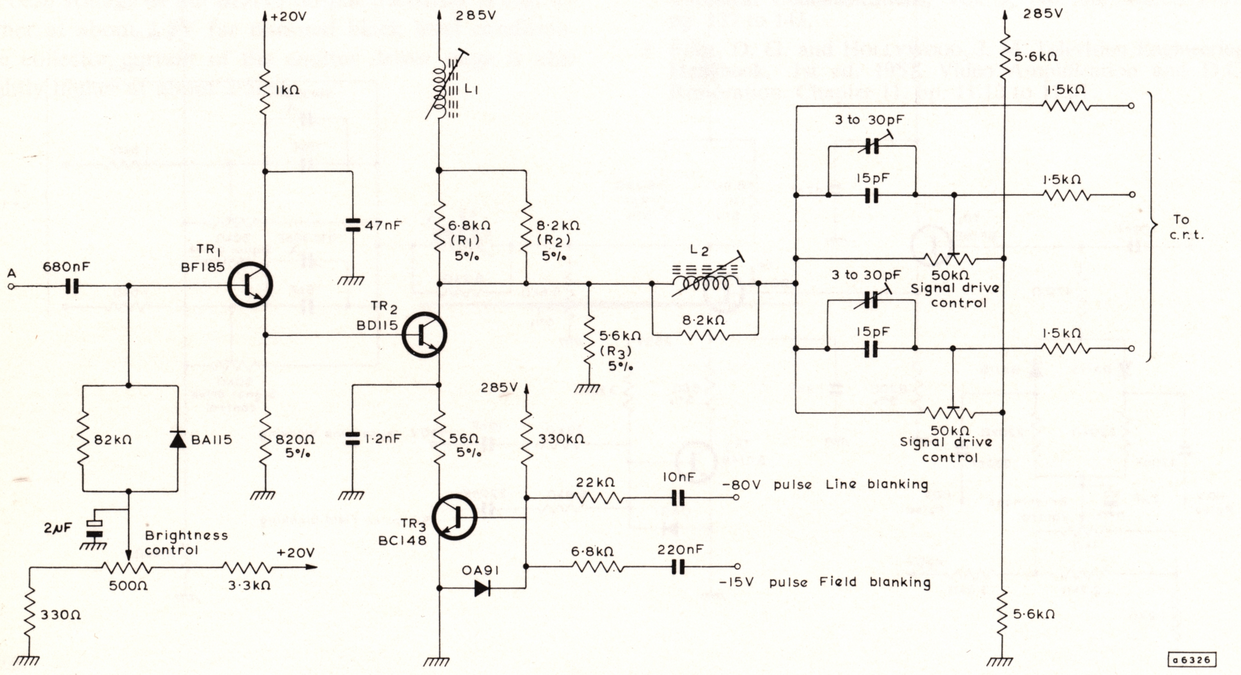
+20V
1kΩ
47nF
A
680nF
TR1
BF185
82kΩ
BA115
2μF
Brightness control
500Ω
3·3kΩ
+20V
330Ω
820Ω 5%
285V
L1
6·8kΩ (R1) 5%
8·2kΩ (R2) 5%
TR2
BD115
5·6kΩ (R3) 5%
1·2nF
56Ω 5%
285V
330kΩ
TR3
BC148
22kΩ
10nF
-80V pulse Line blanking
6·8kΩ
220nF
-15V pulse Field blanking
OA91
L2
8·2kΩ
3 to 30pF
15pF
50kΩ Signal drive control
1·5kΩ
To c.r.t.
5·6kΩ
66326

Fig. 6—Emitter follower driver stage with single-diode d.c. restoration, and BD115 luminance output stage

Operating Conditions of BD115

In the data sheets for the BD115, the maximum dissipation is given as 6W, and a minimum collector to emitter breakdown voltage of 220V is specified. However, the output stage is not designed to accommodate a full 6W dissipation, with a higher than nominal collector voltage, since the heatsink would become abnormally large for a video output stage.

Therefore the collector voltage is set to a similar value as for the BF186, that is 170V for a nominal supply voltage of 285V. Hence from Eq. 1 (page 271), the value of the resistors from collector to earth and h.t. line to collector are respectively 5·46kΩ and 3·71kΩ. In the circuit the resistor values are 5·6kΩ, and 6·8kΩ with 8·2kΩ in parallel, each of 5% tolerance.

To keep the heatsink within manageable proportions it was decided to limit the maximum dissipation to 4W. The preferred values of resistor in the collector load circuit will allow a maximum dissipation of $172^2/4\times 2{\cdot}23\times 10^3 = 3{\cdot}3$W in the transistor for a nominal supply voltage of 285V. For 4W maximum dissipation the highest value of collector voltage to allow for circuit spreads and increases in supply voltage is limited to 190V. In the BD115 the thermal resistance from junction to mounting base is given as 15degC/W. Then assuming a 55°C ambient and junction temperature of 200°C, Eq. 2 (page 272) indicates that the thermal resistance of the heatsink should be about 20degC/W.

Fig. 7 shows the 2·2kΩ load line plotted on the V_{CE}-I_c axes for the BD115. The output voltage conditions are the same as those given for the BF186, that is, 105V black-to-white video signal, 15V blanking and 20V brightness control. The h.f. knee voltage is assumed to be 20V, although the indications are that it is somewhat lower than for the BF186. The voltage drop across the emitter resistor at maximum current will be about 4·5V and the voltage drop due to leakage current is similarly taken as typically 4V.

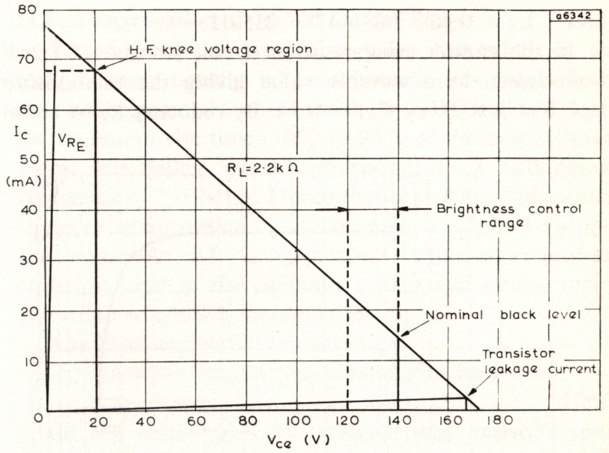

Fig. 7—Operating conditions for BD115 with a 2·2kΩ load resistor

As a similar voltage gain to the BF186 stage is required the effective emitter resistor given approximately by R_L/R_E is 65Ω. Allowing for the equivalent resistance of the bottomed blanking transistor, a 56Ω 5% tolerance resistor is used.

H.F. Compensation of BD115 Output Stage

A similar method to the BF186 circuit shunt-series-peaking and emitter compensation is used for the BD115 output stage. Although the heatsink required is considerably larger, by careful arrangement it is possible to keep the shunt collector capacitance value similar to that of the BF186.

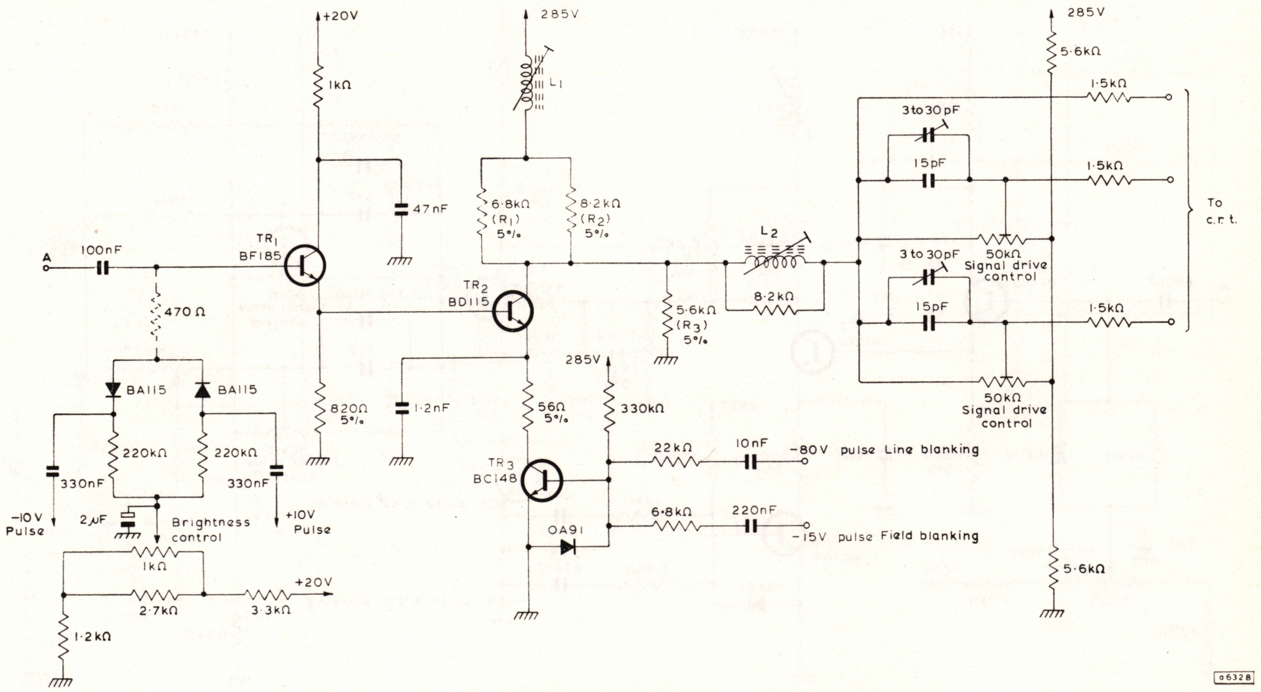

Fig. 8—Emitter follower driver stage with double-diode clamp, and BD115 luminance output stage

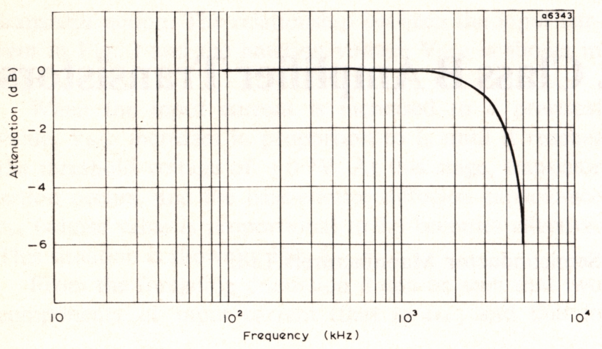

Fig. 9—Frequency response of BD115 output stage

In the uncompensated amplifier with the collector load of 2·2kΩ, the measured rise time was 240ns, corresponding to a 3dB bandwidth of 1·46MHz and hence a total shunt capacitance in the output circuit of 48pF. With similar design factors for m_1 and m_2 the respective values for the shunt and series inductances are $L_1 = 23\mu$H and $L_2 = 107\mu$H. In the practical circuit, the series inductance value was reduced to 70μH, shunted with an 8·2kΩ resistor, and an emitter compensation capacitor of 1·2nF applied. The average measured rise and fall time of the output stage was 85ns corresponding to a 3dB bandwidth of 4·1MHz. Fig. 9 shows the measured frequency response curve indicating a 3dB bandwidth of 4·5MHz.

Emitter Driver Stage and D.C. Restoration

The circuit and operating conditions of this section of the amplifier are similar to the BF186 design, except that the base voltage of the BD115 output transistor is slightly higher at about 1·8V for nominal black level condition. The collector current of the emitter driver stage is also slightly higher at about 2·5mA.

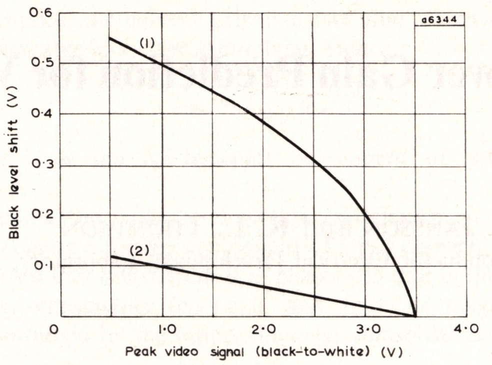

Fig. 10—Comparison of performance of
(1) single-diode d.c. restoration circuit, and
(2) double-diode clamp circuit

SUMMARY

The power limits of the BF186 impose a rather restricted performance in terms of frequency response when used with a 3·3kΩ load. However, under the conditions described maximum drive will be available for the picture tube with some reduction of bandwidth.

Operating the BD115 transistor with the 2·2kΩ collector load at 4W maximum dissipation gives adequate frequency response and luminance drive to the picture tube.

The single-diode d.c. restorer circuit gives a satisfactory performance in the base circuit of the driver transistor, but the double-diode clamp is considerably superior in clamping the black level constant (see Fig. 10).

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Power Gain Prediction for V.H.F. Class B Amplifier Transistors

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The power gain of transistors used in v.h.f. class B amplifiers is predicted from a consideration of device parameters.

INTRODUCTION

The theory of small-signal class A amplifiers operating at v.h.f. is comparatively well known; for class B v.h.f. power amplifiers, however, extension and modification of the class A theory is required. The conventional hybrid-π high frequency equivalent circuit can still be used, provided that two additional elements are included (Fig. 1); these are the base-emitter depletion layer capacitance c_{te} and the emitter lead inductance L_e.

Before the relevance of the equivalent circuit parameters can be determined, it is necessary to understand the operation of the transistor in its application circuit (Fig. 2). Collector efficiencies in the range 60% to 90% are observed with this type of circuit, suggesting that the mode of operation is class B or class C, but examination of the base input current and the base-emitter voltage shows that they are both almost perfectly sinusoidal. Explanation of this apparent anomaly leads to an understanding of the difference between class A and class B operation at v.h.f. and so facilitates the choice of transistor design for a given performance in transmitter applications.

TRANSISTOR ACTION AT V.H.F.

Consider the device equivalent circuit in the greatly simplified form of Fig. 3. It should be remembered, first, that no transistor action can occur until the base-emitter voltage $V_{b'e'}$ reaches the threshold voltage of +0·7V (Fig. 4), and, second, that the capacitance of the emitter diffusion capacitance c_{se} is zero when i_c is 0. It is obvious, therefore, that small sinusoidal input currents can flow in the emitter depletion capacitance c_{te} without causing transistor action. The relationship between the input current in Fig. 3 and the junction voltage $V_{b'e'}$ is shown in Fig. 5.

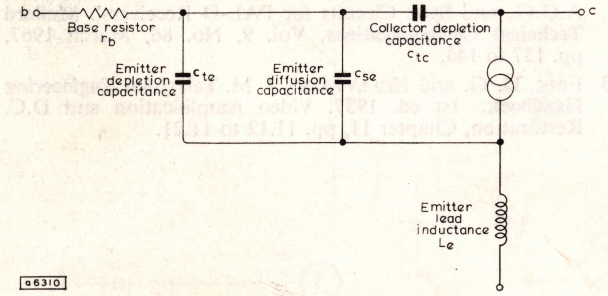

b
Base resistor
r_b
Collector depletion capacitance
c_{tc}
c
Emitter depletion capacitance
c_{te}
Emitter diffusion capacitance
c_{se}
Emitter lead inductance
L_e
a6310

Fig. 1—Hybrid-π equivalent circuit including emitter lead inductances and emitter depletion capacitance

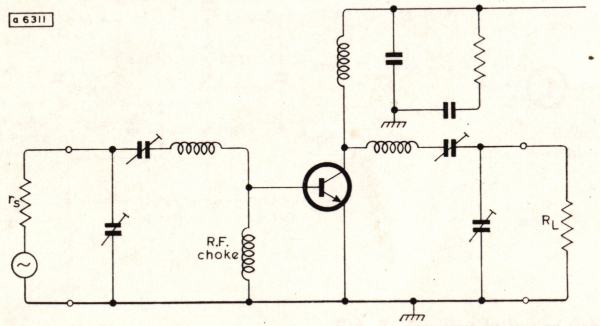


Fig. 2—Typical practical circuit

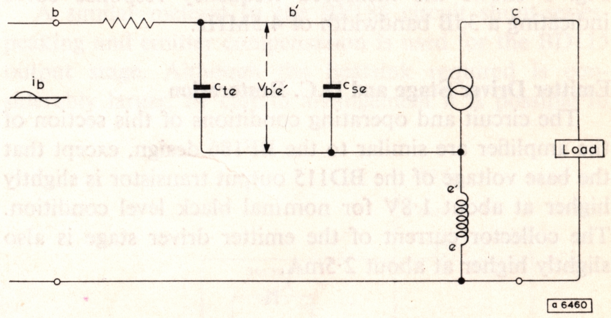


Fig. 3—Simplified equivalent circuit

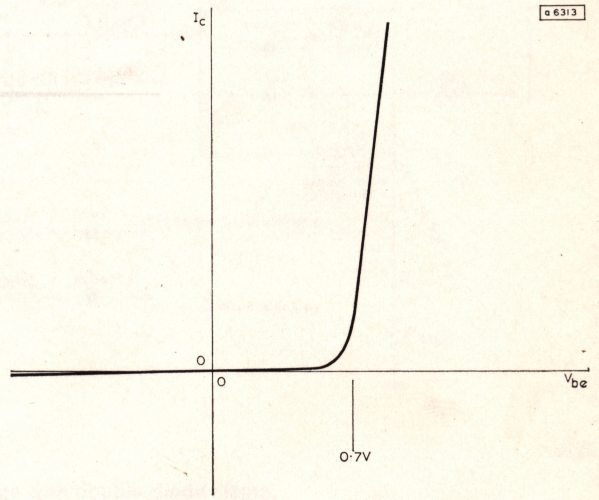


Fig. 4—Junction characteristic

When the input current is increased to a practical value, $V_{b'e'}$ increases in proportion to i_b until it reaches the threshold voltage of +0·7V. At this stage, transistor action occurs, and the base-emitter diffusion capacitance c_{se} (whose value is proportional to I_c) becomes effective. This situation is shown in Fig. 6.

From the foregoing discussion it can be seen that two components of input current (that in c_{te}, and that in c_{se}) must be taken into account. The current $i_{c_{te}}$ in c_{te} is given by the following equation, where c_{te} is measured at zero voltage.

$$i_{c_{te}} \simeq 0{\cdot}7\omega c_{te}. \qquad \ldots(1)$$

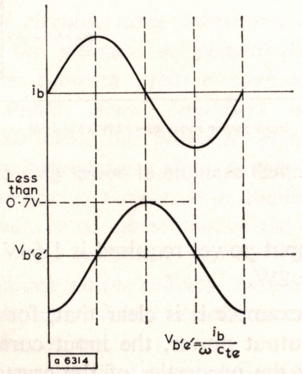
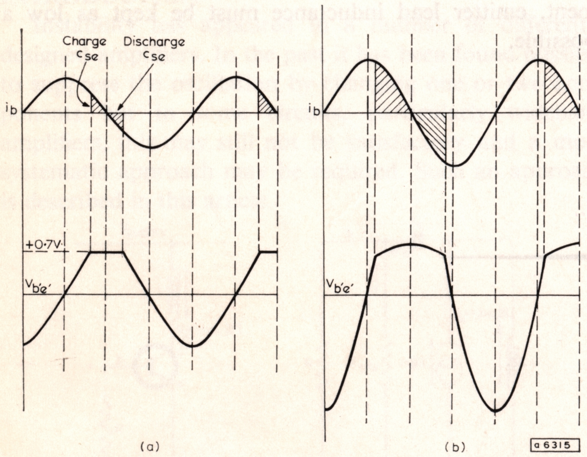


Fig. 5—Relationship between input current and junction voltage for values of $V_{b'e'}$ less than 0·7V



(a) (b)

Fig. 6—Relationship between input current and junction voltage
(a) for very low input powers
(b) for normal input powers

The 0·7V is taken as the r.m.s. value to give a close approximation to the input current required to charge c_{te} to approximately 0·7V during a half-cycle, as indicated in Fig. 6b.

Because the conduction angle for normal operation is approximately 90° (Fig. 6), and because half of the total input current in Fig. 3 is lost in the emitter depletion capacitance, the current gain is a half that which would be applicable in a class A amplifier. Hence,

$$i_{c_{se}} = 2.\frac{f}{f_T}.i_c\,, \qquad \ldots(2)$$

where i_c is the fundamental component of collector current.

Adding the collector depletion capacitance c_{tc} (as in Fig. 7) gives a further component of input current. It can be shown that this current is in phase with that in the total emitter capacitance ($c_{te}+c_{se}$), and since its magnitude is determined by the (approximately) sinusoidal collector voltage, its value can be easily calculated, if it is assumed that the voltage swing at the base end of c_{tc} is small enough to be ignored.

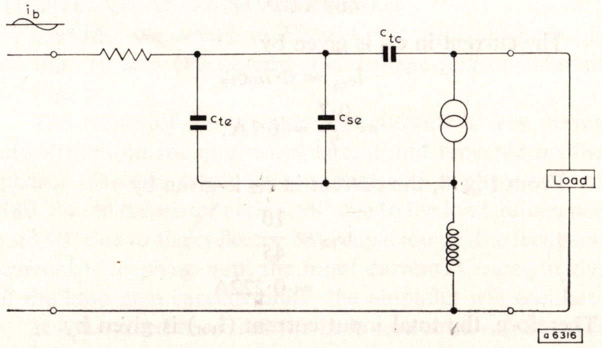


Fig. 7—Equivalent circuit with collector depletion layer capacitance included

It will be observed that the only power loss in the input circuit is in the base resistance, whose effective value must be assessed for the particular case of class B operation. The total input power required is however considerably greater than that lost in r_b. This is because the voltage dropped across L_e (due to the fundamental component of current produced by the current generator) is in phase with the input current.

ILLUSTRATIVE CALCULATION

If the desired load power is known, the relevant currents and voltages in the circuit to be calculated, and the power gain, can be determined. Conversely, a given power gain requirement enables one to obtain many combinations of device parameters which could give the desired performance. This may be illustrated by means of a practical example.

Let the circuit conditions be:

Required output power = 10W
Frequency = 175MHz
Supply voltage = 14·1V

Assume the transistor parameters to be as follows:

f_T = 400MHz
c_{tc} = 20pF (= 45Ω)
c_{te} = 130pF (= 7Ω)
L_e = 1·27nH (= 1·4Ω)
r_b = 0·2Ω

To calculate the input power required, it is only necessary to consider the relevant in-phase fundamental components: the calculation is illustrated in Fig. 8.

The peak voltage swing at the collector is equal to the supply voltage (14·1V). Therefore the r.m.s. value of collector voltage is 10V. For an output power of 10W, the load resistance required will therefore be (10^2/10) or 10Ω. The collector current will thus be (10/10) or 1A.

From Eq. 2, the current in c_{se} is given by

$$i_{c_{se}} = 2.\frac{f}{f_T}.i_c\,,$$

that is,

$$i_{c_{se}} = 2\times\frac{175\times10^6}{400\times10^6}\times1 = 0{\cdot}875\text{A}.$$

The current in c_{te} is given by

$$i_{c_{te}} = 0{\cdot}7\omega c_{te}$$

$$= \frac{0{\cdot}7}{7} = 0{\cdot}1\text{A}.$$

From Fig. 8, the current in c_{tc} is given by

$$i_{c_{tc}} = \frac{10}{45}$$

$$= 0{\cdot}222\text{A}$$

Therefore, the total input current (I_{tot}) is given by

$$I_{tot} = 0{\cdot}875+0{\cdot}1+0{\cdot}222$$

$$\simeq 1{\cdot}2\text{A}.$$

Thus, the voltage across r_b

$$= 0{\cdot}2\times1{\cdot}2 = 0{\cdot}24\text{V}.$$

Again, it can be seen from Fig. 8 that the relevant component of current in L_e which will produce across L_e a voltage in phase with the input current, is 1A. Therefore the voltage across L_e is 1·4V. Consequently, the total input voltage is 0·24V+1·4V, that is, 1·64V.

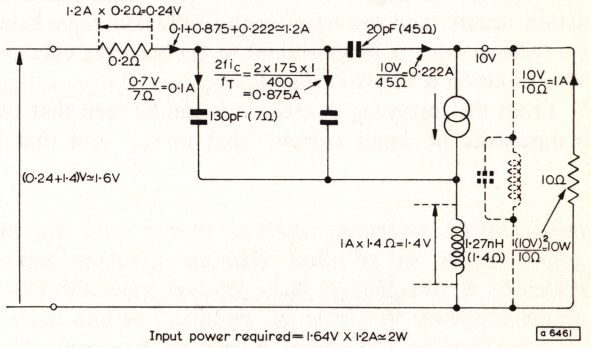

1·2A x 0·2Ω=0·24V
0·1+0·875+0·222≃1·2A
20pF (45Ω)
0·2Ω
10V
2fic/fT = 2x175x1/400 =0·875A
0·7V/7Ω=0·1A
10V/45Ω=0·222A
10V/10Ω=1A
130pF (7Ω)
(0·24+1·4)V≃1·6V
10Ω
1A x 1·4Ω=1·4V
1·27nH (1·4Ω)
(10V)²/10Ω=10W
Input power required=1·64V X 1·2A≃2W
a 6461

Fig. 8—Practical example of power gain calculation

Thus the input power required is 1·64V×1·2A, that is, approximately 2W.

From this example it is clear that, for a given supply voltage and output power, the input current required is determined by the properties of the crystal, whereas the input voltage is almost directly proportional to the emitter lead inductance. It follows therefore that, in the design of the device encapsulation and in the design of the equipment, emitter lead inductance must be kept as low as possible.

Parasitic Oscillations in V.H.F. Power Amplifiers

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In a variety of circuits, using transistors as v.h.f. power amplifiers for the ultimate or penultimate stages of a transmitter, the common emitter configuration is only conditionally stable. Some amplifiers with transistors operating in this mode are prone to oscillate; the most troublesome oscillations take place at less than the signal frequency and appear at the output as amplitude modulation of the r.f. output, or as modulation of the mean r.f. level.

The cause of the instability can be traced in the first instance to feedback via the collector base capacitance from the output to the input. Under certain circuit conditions the feedback may be positive.

A theory to explain some types of instability is suggested and practical methods of stabilising a wideband amplifier are discussed.

INTRODUCTION

Instability has appeared in a number of differently designed amplifiers. In the past it has been found possible to suppress the oscillation by changing one or two components but in some circuits, particularly wideband amplifiers, this may still not be satisfactory and a more systematic approach may be required. Such an approach is described in this article.

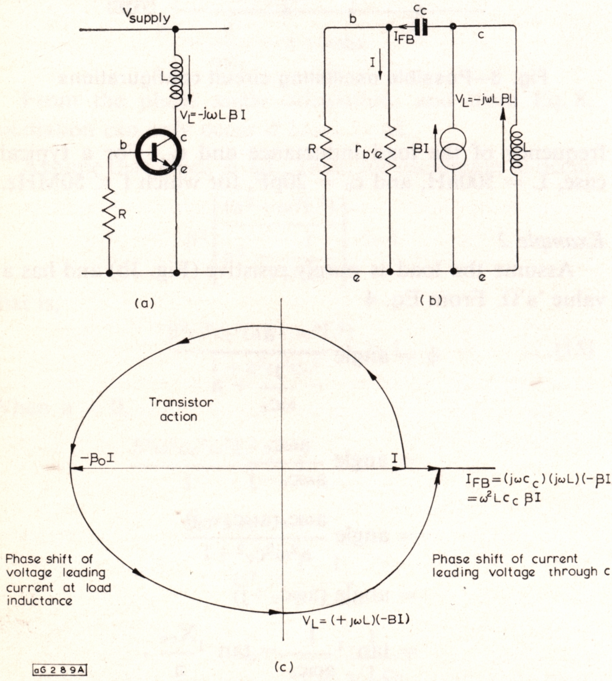
Vsupply
L
VL=-jωLβI
b
c
e
R
(a)
cc
b
IFB
c
I
VL=-jωLβL
R
rb'e
-βI
L
e
e
(b)
Transistor action
-βoI
I
IFB=(jωcc)(jωL)(-βI)
=ω²LccβI
Phase shift of voltage leading current at load inductance
Phase shift of current leading voltage through cc
VL=(+jωL)(-βI)
aG289A
(c)

Fig. 1—Circuit under consideration, together with the equivalent circuit and phasor diagram

THEORETICAL FUNDAMENTALS

Consider the circuit of Fig. 1a, the equivalent circuit of Fig. 1b and the current and voltage phasor diagram of Fig. 1c.

The values of the voltages and currents at key points are written on the equivalent circuit and repeated on the phasor diagram. It can be seen that with a phase shift of 180° due to transistor action, 90° due to the load inductance and 90° due to the collector base capacitance, the feedback current is in phase with the input current. Consequently, if the loop gain exceeds unity, the amplifier will oscillate.

It is assumed here that the base resistance $r_{bb'}$ is small and that the reactance of c_e is very much greater than the base to emitter resistance $r_{b'e}$. For the purpose of the above illustration the depletion capacitance of the base-emitter junction is ignored. The load L is assumed to be a pure inductance.

The General Case

Consider the circuit of Fig. 2a and the equivalent circuit of Fig. 2b, and consider an initial current I at a given frequency. If the current gain at this frequency is β and the feedback current to the input is I_{FB}, the voltage V_L appearing across the load is given by

$$V_L = Z_L(-\beta I - I_{FB}). \qquad \ldots(1)$$

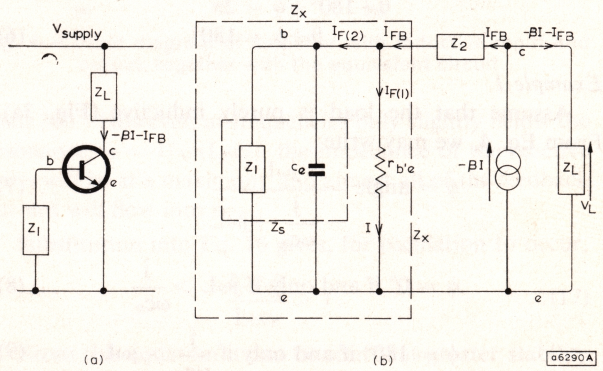
Vsupply
ZL
-βI-IFB
b
c
e
Z1
Zx
b
IF(2)
IFB
Z2
IFB
-βI-IFB
c
IF(1)
Z1
ce
rb'e
-βI
ZL
VL
Zs
I
Zx
e
e
(a)
(b)
a6290A

Fig. 2—Circuit under consideration and its equivalent circuit

Let Z_x be the total input impedance, that is, Z_1 in parallel with the transistor impedance.

Then

$$I_{FB} = Z_x + Z_2 = V_L$$

$$= Z_L(-\beta I - I_{FB}).$$

Therefore

$$I_{FB} = \frac{-\beta I Z_L}{Z_x+Z_2+Z_L}.$$

Generally, Z_x is small compared with Z_2+Z_L. Typical values for the components of Fig. 2b are $Z_2 < 20\text{pF}$, $c_e = 150\text{pF}$ in the off condition, $c_e \gg 150\text{pF}$ in the on condition, and $r_{b'e} \simeq 10\Omega$ for $I_E = 200\text{mA}$. Therefore we may write,

$$I_{FB} = \frac{-\beta I Z_L}{Z_2+Z_L}. \qquad \ldots(2)$$

Let Z_S be the impedance of the parallel combination (Fig. 2b) of Z_1 and c_e. Then

$$I_{F(2)}Z_S = r_{b'e}I_{F(1)}\,,$$

whence

$$\frac{I_{F(1)}}{I_{F(2)}} = \frac{Z_S}{r_{b'e}}$$

$$\frac{I_{F(1)}}{I_{F(1)}+I_{F(2)}} = \frac{Z_S}{r_{b'e}+Z_S}.$$

But

$$I_{F(1)}+I_{F(2)} = I_{FB}.$$

Therefore

$$I_{F(1)} = I_{FB}.\frac{Z_S}{r_{b'e}+Z_S}\,. \qquad \ldots(3)$$

Substitution in Eq. 2 gives

$$\frac{I_{F(1)}}{I} = \left[\frac{Z_S}{r_{b'e}+Z_S}\right]\times\left[-\beta\right]\times\left[\frac{Z_L}{Z_2+Z_L}\right]. \qquad \ldots(4)$$

Conversion to modulus and angle gives

$$\frac{I_{F(1)}}{I} = [A \text{ angle } \theta]\times[\beta \text{ angle } 180]\times[C \text{ angle } \phi]. \qquad \ldots(5)$$

For oscillation, $I_{F(1)}$ must be in phase with I, and $(I_{F(1)}/I)$ must exceed unity.

Phase Angle

For oscillation, angle $\frac{I_{F(1)}}{I} = 2n\pi$ where n is an integer.

That is,

$$\theta+180^\circ+\phi = 2\pi$$

$$\theta+\phi = 180^\circ. \qquad \ldots(6)$$

Example 1

Assume that the load is purely inductive (Fig. 3a). From Eq. 4, we may write

$$\phi = \text{angle}\,\frac{j\omega L}{-\frac{j}{\omega c_c}+j\omega L} \qquad \ldots(7)$$

$$\phi = 0^\circ \text{ if and only if } j\omega L > \frac{j}{\omega c_c} \qquad \ldots(8)$$

$$\phi = 180^\circ \text{ if and only if } \frac{j}{\omega c_c} > j\omega L. \qquad \ldots(9)$$

Substitution in Eq. 6 gives

$$\text{For oscillation } \theta+0 = 180^\circ \qquad \ldots(10)$$

or

$$\text{For oscillation } \theta+180^\circ = 180^\circ. \qquad \ldots(11)$$

Eq. 10 gives

$$\theta = 180^\circ, \qquad \ldots(12)$$

which, from Eq. 4, is not possible. Thus we must take the solution from Eq. 11, that is

$$\theta = 0. \qquad \ldots(13)$$

We may then write

$$\text{angle}\,\frac{Z_S}{r_{b'e}+Z_S} = 0.$$

This is true when Z_S is purely real, that is, when the parallel combination of the external circuit and c_e is purely resistive. (This confirms the assumption made earlier in the discussion of Fig. 1, illustrating the principle that oscillation can occur if the load is purely inductive and the input resistive). However, oscillation in this mode is only possible if Eq. 8 is satisfied. That is,

$$\frac{1}{\omega c_c} > \omega L$$

whence

$$1 > \omega^2 L c_c$$

$$\omega < \frac{1}{\sqrt{(Lc_c)}}. \qquad \ldots(14)$$

The oscillation frequency is below the resonance frequency of the load inductance and c_c. For a typical case, $L = 500\text{nH}$, and $c_c = 20\text{pF}$, for which $f < 50\text{MHz}$.

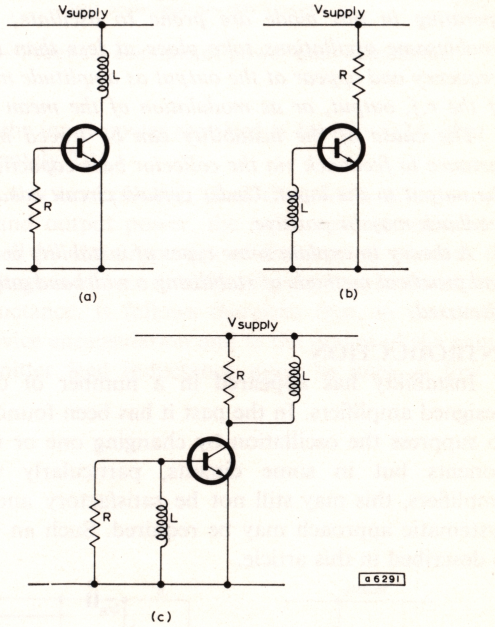

Fig. 3—Possible oscillating circuit configurations

Example 2

Assume the load is purely resistive (Fig. 3b) and has a value 'a'Ω. From Eq. 4

$$\phi = \text{angle}\,\frac{a}{-\frac{j}{\omega c_c}+a}$$

$$= \text{angle}\,\frac{a\omega c_c}{a\omega c_c - j}$$

$$= \text{angle}\,\frac{a\omega c_c(a\omega c_c+j)}{a^2\omega^2 c_c^2+1}$$

$$= \text{angle}\,(a\omega c_c+j)$$

$$= \tan^{-1}\frac{1}{a\omega c_c} = \tan^{-1}\frac{X_{cc}}{a}\,,$$

where X_{cc} is the reactance of the collector base capacitance.

The value of ϕ tends to 90° as X_{cc} becomes very much greater than 'a'. Substitution in Eq. 6 gives

$$\theta+90 = 180^\circ,$$

that is,

$$\theta = 90^\circ.$$

In the limit, when ϕ has tended to 90°, it is possible for the circuit to oscillate if the output is resistive and the input is purely inductive and if the loop gain is greater than 1. See Fig. 3b.

Example 3

It is also possible that oscillation can occur with intermediate phase angles in the input and output (Fig. 3c).

Loop Gain

For oscillation to occur, we may write from Eq. 5.

$$A\beta C > 1$$

that is

$$\left|\frac{Z_S}{r_{b'e}+Z_S}\right|\times\left|\beta\right|\times\left|\frac{Z_L}{-\frac{j}{\omega c_c}+Z_L}\right| > 1.$$

If $r_{b'e}$ is very much less than Z_S, which is the normal condition, then

$$\frac{Z_S}{r_{b'e}+Z_S}\text{tends to 1.}$$

This represents the worst case condition when all the feedback current passes into the base of the transistor.

$$\text{Loop gain} = \beta\left|\frac{Z_L}{-\frac{j}{\omega c_c}+Z_L}\right|.$$

If $Z_L = a+j\omega L$, then, for oscillation to occur

$$\beta\left|\frac{a+j\omega L}{-\frac{j}{\omega c_c}+a+j\omega L}\right| > 1.$$

From the phase angle calculation, and from Eq. 8, oscillation can only occur if $1/\omega c_c > \omega L$.

Assume that $1/\omega c_c \gg \omega L$. Then, for oscillation to occur

$$\beta^2\left[\frac{(a^2+\omega^2L^2)}{a^2+\frac{1}{\omega^2 c_c^2}}\right] > 1$$

that is,

$$\frac{\beta^2\omega^2 c_c^2(a^2+\omega^2L^2)}{1+a^2\omega^2c_c^2} > 1. \qquad \ldots(15)$$

When a = 0,

$$\frac{\beta^2\omega^2c_c^2\omega^2L^2}{1} > 1$$

$$\beta\omega^2Lc_c > 1$$

$$\omega^2 > \frac{1}{\beta}.\frac{1}{Lc_c}$$

$$\omega > \frac{1}{\sqrt{\beta}}.\frac{1}{\sqrt{Lc_c}}.$$

This gives the lowest frequency of oscillation, and indicates that the assumption that $1/\omega c_c \gg \omega L$ is justified except for large values of collector load inductance.

Thus, if $L = 30\mu\text{H}$, and if $c_c = 20\text{pF}$, and if $\beta = 100$, then $f > 600\text{kHz}$.

Design with Chokes

Consider Figs. 4a and 4b which show a transistor with collector and base bias chokes only. Following the general theory outlined above, and assuming that the feedback current is small compared with the load current, then

$$V_L \simeq -\,j\omega L_c\beta i,$$

and the feedback current is given by

$$i_{FB} \simeq -\,j\omega L_c\beta i(j\omega c_c)$$

or

$$i_{FB} \simeq \omega^2 L_c c_c \beta i.$$

For oscillation to occur

$$i_{FB} > i$$

or

$$\omega^2 L_c c_c \beta > 1. \qquad \ldots(16)$$

Oscillation cannot take place above the resonant frequency of the base choke and the emitter depletion capacitance since the total phase shift would then be less than 360°. However, at frequencies only slightly below the resonance, $\omega = 1/\sqrt{(L_b c_e)}$, the impedance of the reactive parts will be at a maximum, and almost all of the feedback current will flow into $r_{b'e}$.

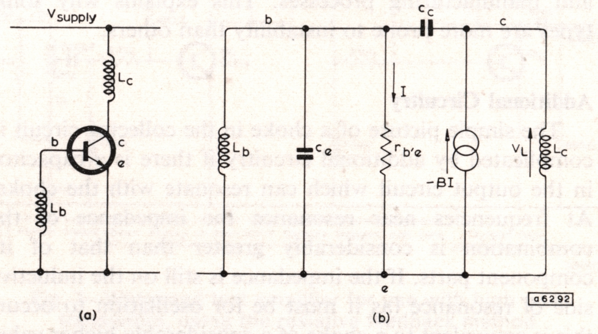

Fig. 4—Circuit diagram of amplifier with inductive input and output, together with the equivalent circuit

Substitution into Eq. 16 gives, for oscillation to occur,

$$\frac{L_c c_e \beta}{L_b c_e} > 1. \qquad \ldots(17)$$

From this equation it can be seen that greater stability will be achieved if the collector choke is smaller than the base choke.

THEORY AND PRACTICE OF POSSIBLE CURES

Various practical methods of avoiding oscillation are now discussed under separate headings.

Supply Decoupling

Difficulties have been encountered, in practice, with resonances between the supply decoupling capacitors and inductances both in the circuit and in the supply lines. Resonances have also been noticed between undamped capacitors in parallel. A 'preferred' circuit was designed

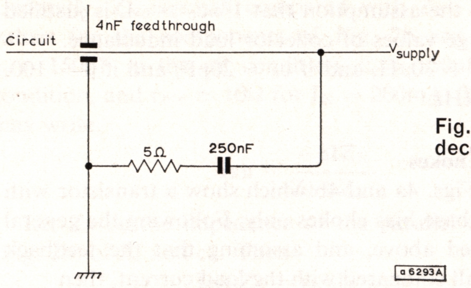

Fig. 5—Preferred decoupling circuit

and has proved very satisfactory in use (Fig. 5). At frequencies above 100kHz the impedance is less than $(5-5j)\Omega$.

It has been found that a great number of parasitic oscillation problems can be traced to inadequate or unsatisfactory supply decoupling.

Design with Chokes

From the above discussion concerning chokes (and in particular from Eq. 17), it can be seen that stability can be improved by making the base choke larger than the collector choke. Little can be done with β, c_c and c_e as these factors are primarily dependent on device geometry and manufacturing processes. This explains why some types are more prone to instability than others.

Additional Circuitry

The simple picture of a choke in the collector circuit is complicated by additional circuitry if there is a capacitor in the output circuit which can resonate with the choke. At frequencies near resonance the impedance of the combination is considerably greater than that of its component parts. If the impedance is still on the inductive side of resonance (as it must be for oscillation to occur) this is equivalent to a choke of a considerably higher value than that in situ and oscillation may occur as described previously. The impedance which may be seen at the collector is dependent on the Q of the circuit. Under fault conditions the Q may be very high and it has sometimes been found helpful to limit the Q by including a fixed resistor across the output. This does not affect the performance significantly if it is at least 15 times higher than the matched impedance.

On the input side a low value of inductance connected to ground may shunt the base choke entirely and oscillation may occur by Eq. 17 if the effective L_b is low enough.

From Eq. 4 it can be seen that it would be advantageous to decrease the value of $Z_S/(r_{b'e}+Z_S)$ where Z_S is the impedance of the input circuitry together with c_e. This may be done satisfactorily by a low value resistor connected between base and ground. However, power will be lost in this resistor and its effectiveness depends on the relative magnitudes of $r_{b'e}$ and Z_S.

Phase Control Method

Because of radiation, resistance, small losses in components, etc., the phase shift in either the input or output circuits singly can never quite reach 90°. If now one side (either the input or output) is prevented from becoming inductive, or is always slightly capacitive, the phase shift round the loop will never quite reach 360°. Consequently, oscillation cannot occur, as Eq. 6 indicates.

If oscillation is troublesome in the output stage, phase control must be applied to the input circuit since under fault conditions, with an aerial attached, the output impedance may take any value, capacitive or inductive. This solution limits circuit design considerably and it can be very difficult in practice to make a circuit capacitive at all frequencies, because of imperfections in components at high frequencies. Thus, capacitors may look inductive and inductances may look capacitive.

An example of the use of this method is shown in Fig. 6, which shows a wideband output circuit of a small transmitter, using a high gain development transistor in the output stage.

In practice, a selection of filters was necessary in the output, and under fault conditions, the possible values of impedances at the collector could take on any value. The coupling circuit between the transistor stages was designed to give a satisfactory gain as well as to remain capacitive at all frequencies. One difficult compromise had to be made between the collector choke of the first stage and the base choke of the second stage. For stability of the first stage the collector choke had to be as small as possible but for the stability of the second stage the base choke had to be as large as possible. They were coupled with 1nF and it was only by adjustment of this coupling capacitor, and by the choice of the base-to-emitter resistor-capacitor combination, that satisfactory stability was achieved.

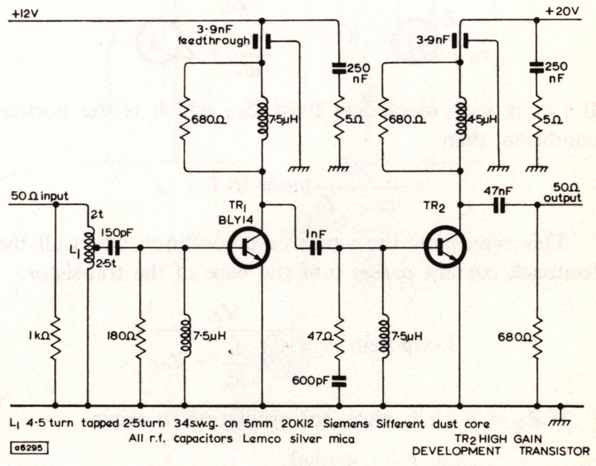
+12V
+20V
3·9nF feedthrough
250 nF
3·9nF
250 nF
680Ω
7·5μH
5Ω
680Ω
45μH
5Ω
50Ω input
2t
150pF
L1
25t
TR1 BLY14
1nF
TR2
47nF
50Ω output
1kΩ
180Ω
7·5μH
47Ω
7·5μH
600pF
680Ω
L1 4·5 turn tapped 2·5turn 34s.w.g. on 5mm 20K12 Siemens Sifferent dust core
All r.f. capacitors Lemco silver mica
TR2 HIGH GAIN DEVELOPMENT TRANSISTOR
a6295

Fig. 6—Wideband test amplifier for use with high gain transistors, using the phase control method to suppress oscillation

Resistor Feedback Method

A second method of stabilisation of a development circuit was the use of a feedback resistor connected between the collector and base of each oscillating transistor. This has the effect of 'swamping' the collector base capacitance and prevents the phase shift from reaching 360°.

The calculation of the value of the resistance required is shown below. From Eq. 4,

$$\frac{I_{F(1)}}{I}=\left[\frac{Z_S}{r_{b'e}+Z_S}\right]\times\left[-\beta\right]\times\left[\frac{Z_L}{Z_2+Z_L}\right].$$

Assume under worst case conditions, that all the feedback current returns to the transistor base. Then

$$\frac{Z_S}{r_{b'e}+Z_S}=1, \qquad \ldots(18)$$

and

$$\frac{I_{F(1)}}{I}=-\beta.\frac{Z_L}{Z_2+Z_L}. \qquad \ldots(19)$$

With a resistor connected from collector to base, then Z_2 (from Fig. 2b) has the value of R in parallel with c_c. That is,

$$\frac{1}{Z_2}=j\omega c_c+\frac{1}{R}$$

$$Z_2=\frac{R}{1+j\omega c_c R}$$

$$=\frac{R(1-j\omega c_c R)}{1+\omega^2 c_c^2 R^2}.$$

Substitution in Eq. 19 gives

$$\frac{I_{F(1)}}{I}=\frac{-\beta Z_L(1+\omega^2 c_c^2 R^2)}{R(1-j\omega c_c R)+Z_L(1+\omega^2 c_c^2 R^2)}.$$

Let $Z_L=j\omega L$, which is the most likely condition for oscillation. Then

$$\frac{I_{F(1)}}{I}=\frac{-j\beta\omega L(1+\omega^2 c_c^2 R^2)}{R+j(\omega L+\omega^3 L c_c^2 R^2-\omega c_c R^2)}.$$

Therefore

$$\frac{I_{F(1)}}{I}$$

$$=\frac{[-j\beta\omega L(1+\omega^2 c_c^2 R^2)][R-j(\omega L+\omega^3 L c_c^2 R^2-\omega c_c R^2)]}{R+j(\omega L+\omega^3 L c_c^2 R^2-\omega c_c R^2)}.$$

For simplicity, say

$$\frac{I_{F(1)}}{I}=A+jB.$$

For complete stability A should ideally be negative.

That is,

$$\beta\omega L(1+\omega^2 c_c^2 R^2)(\omega L+\omega^3 L c_c^2 R^2-\omega c_c^2 R^2)>0$$

or

$$L+\omega^2 L c_c^2 R^2>c_c R^2.$$

Therefore

$$R^2(c_c-\omega^2 L c_c^2)<L$$

$$R^2<\frac{L}{c_c-\omega^2 L c_c^2}.$$

The minimum value of R occurs when ω tends to 0, that is, when $R^2<L/c_c$.

Hence, the maximum resistance allowed for complete stability is $\sqrt{(L/c_c)}$.

Example 4

Assuming a minimum collector inductance of 5μH and c_c of 20pF,

$$R<\sqrt{\left(\frac{5\times10^{-6}}{20\times10^{-12}}\right)}$$

$$R<\tfrac{1}{2}\times10^3$$

$$R<500\Omega.$$

Two obvious disadvantages of this system are d.c. current shunting and loss of gain. By judicious choice of values a capacitor may be included in series with the resistor to block the d.c. current with no detrimental effect, provided that its value is chosen so that the combination is not significantly capacitive at the lowest troublesome frequency.

If the oscillation frequency is different from the drive frequency then it is possible to include a choke in series with the combination. This reduces the loss at the operating frequency but has little effect at the lower frequency. Restraint should be exercised in using this solution, however, since it is possible to have oscillation with capacitive input, capacitive output and inductive feedback. Fig. 7 shows an example of a circuit using the technique of resistive feedback.

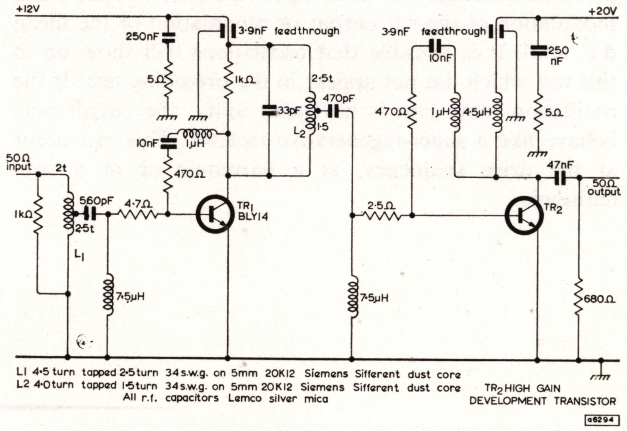
+12V
+20V
250nF
3·9nF feedthrough
3·9nF feedthrough
10nF
250 nF
5Ω
1kΩ
2·5t
33pF
470pF
L2
15
470Ω
1μH
45μH
5Ω
10nF
1μH
470Ω
50Ω input
2t
1kΩ
560pF
25t
L1
4·7Ω
TR1 BLY14
2·5Ω
47nF
50Ω output
TR2
7·5μH
7·5μH
680Ω
L1 4·5 turn tapped 2·5turn 34s.w.g. on 5mm 20K12 Siemens Sifferent dust core
L2 4·0turn tapped 1·5turn 34s.w.g. on 5mm 20K12 Siemens Sifferent dust core
All r.f. capacitors Lemco silver mica
TR2 HIGH GAIN DEVELOPMENT TRANSISTOR
a6294

Fig. 7—Wideband test amplifier for use with high gain transistors, using the resistive feedback method to suppress oscillation

SYMPTOMS AND DIAGNOSIS OF OSCILLATIONS

Oscillations which occur under various circuit conditions are discussed under separate headings below. Cures for the oscillation are suggested in each case.

Oscillation with D.C. Supply Only (Class B Stages)

Oscillations may be observed with an oscilloscope connected between earth and the circuit side of the resistor in the preferred decoupling circuit (Fig. 5). However, it is more satisfactory to connect the probe to the collector pin. If any oscillation is observed, the frequency should be noted and the loop gain calculated. Steps can then be taken either by altering component values or by applying solutions discussed in the previous section.

Oscillation with Forward Bias on the Base

The gain of forward biased transistors is relatively greater than that of the transistors in class B or class C stages, and oscillations may occur which did not appear under the previous heading. The application of forward bias also changes the values of c_e and $r_{b'e}$, and an oscillation may start when, in contrast, in an undriven class B stage, the V_{be} (which is approximately 0·7V) would normally prevent oscillation. Cures for this form of oscillation may be attempted by applying the solutions discussed previously.

Oscillation with R.F. Input

Parasitic Frequency Unchanged with Change of Drive Frequency

Since the r.f. drive effectively sweeps the d.c. characteristic, any form of oscillation not cured under the two previous headings will show up in the form of amplitude modulation of the r.f. output or modulation of the mean d.c. level. It is possible that oscillations will show up in this test which did not appear in the preceding test. If the oscillation loop gain is not quite unity, the circuit may behave like a super-regenerative receiver. This can occur at the drive frequency, at a harmonic or at a subharmonic.

Frequency of Oscillation Changes with Change of Drive Frequency

If a circuit is oscillating at one frequency and the drive is at a different frequency, mixing will occur between the two and an oscillation will appear at the difference frequency. Small changes in the drive frequency thus cause a fairly large change in the difference frequency. This type of oscillation has been called 'parametric oscillation' and it occurs more readily in amplifiers where the signal frequency is relatively high, for example, 175MHz.

A cure must be effected by stopping the oscillation at the 'local oscillator' rather than trying to cure the oscillation at the difference frequency. Because the oscillation frequency may be near the signal frequency, it can be difficult to apply some of the cures previously discussed, without a loss of gain.

OTHER FORMS OF OSCILLATION

The preceding is not a complete coverage of parasitic oscillations. One additional, fairly commonly observed form occurs when the transistor is driven hard with a particular fault condition on the output, and the collector-base junction becomes forward biased preventing the transistor operating correctly over the next few cycles. This has been called 'the skip-effect'. Varactor multiplication is not discussed because it is a completely different form of oscillation.

See next issue (Jan. 1968) p. 5-6